IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Shrenik Deliwala	:	
	:	Attorney Docket No.: 53168-500301D3
Serial No.: Not yet known	:	
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Filed: February 15, 2002	:	
	:	
For: INTEGRATED OPTICAL/ELECTRONIC CIRCUITS AND ASSOCIATED METHODS OF SIMULTANEOUS GENERATION THEREOF	:	

PRELIMINARY AMENDMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Prior to the examination of this matter, please amend this application as follows:

EXPRESS MAIL CERTIFICATE (37 C.F.R. § 1.10)

Express Mail Label No. EL931061769US Date of Deposit February 15, 2002

I hereby certify that this paper, and the papers and/or fees referred to herein as transmitted, submitted or enclosed, are being deposited with the U.S. Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Name Daniel H. Golub Signature

IN THE CLAIMS

Please delete claims 1-11 and add new claims 12-57 as follows:

12. A computer implemented device that simulates the electronic and optical characteristics of an integrated optical/electronic circuit, comprising:

an electronic design portion that simulates characteristics of at least certain electronic circuits of said integrated optical/electronic circuit, and generates topology information and free-carrier concentration information associated with the electronic circuits; and

an optical design portion that simulates characteristics of at least certain optical circuits of said integrated optical/electronic circuit in response to said topology information and said free-carrier concentration information generated by said electronic design portion.

13. The device of claim 12, wherein the electronic design portion includes a process simulation portion that generates said topology information.

14. The device of claim 12, wherein the electronic design portion includes a device simulation portion that generates said free-carrier concentration information.

15. The device of claim 12, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

16. The device of claim 12, wherein said optical simulation portion further comprises at

least one of the group consisting of: a waveguide grating portion, a diffraction optical element portion, a finite difference time domain portion, a thin film portion, a beam propagation method portion, and a raytracing portion.

17. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a focusing mirror.

18. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a waveguide.

19. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a Fabry-Perot cavity.

20. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a wavelength division multiplexer modulator.

21. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as an evanescent coupler.

22. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a diode.

23. The device of claim 12, wherein the computer-implemented device simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a transistor.

24. The device of claim 12, wherein the integrated optical/electronic circuit is at least partially formed on a Silicon-On-Insulator (SOI) substrate.

25. The device of claim 24, wherein the topology information generated by the electronic design portion is generated from process limitations.

26. The device of claim 25, wherein said SOI substrate includes a substrate layer, and wherein said waveguide at least partially extends within said substrate layer.

27. The device of claim 12, wherein the optical design portion models one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

28. A computer-readable medium having stored therein a plurality of instructions, the plurality of instructions including instructions which, when executed by a computer processor, simulate the electrical characteristics and the optical characteristics of an integrated optical/electronic circuit, the computer software causing the computer processor to:

simulate, with an electronic design portion, operation of at least certain electronics

circuits of said integrated optical/electronic circuit, said electronic design portion generating topology information and free-carrier concentration information; and

simulate, with an optical simulation portion, operation of at least certain optical circuits of said integrated optical/electronic circuit in response to said topology information and said free-carrier concentration information generated by said electronic design portion.

29. The computer-readable medium of claim 28, wherein the electronic design portion includes a process simulation portion that generates said topology information.

30. The computer-readable medium of claim 28, wherein the electronic design portion includes a device simulation portion that generates said free-carrier concentration information.

31. The computer-readable medium of claim 28, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

32. The computer-readable medium of claim 28, wherein said optical design portion further comprises at least one of the group consisting of: a waveguide grating portion, a diffraction optical element portion, a finite difference time domain portion, a thin film portion, a beam propagation method portion, and a raytracing portion.

33. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as a focusing

mirror.

34. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a waveguide.

35. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a Fabry-Perot cavity.

36. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a wavelength division multiplexer modulator.

37. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including an evanescent coupler.

38. The computer-readable medium of claim 28, wherein the processor simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a diode.

39. The computer-readable medium of claim 28, wherein the processor simulates the

operation of the optical characteristics of an integrated optical/electronic circuit as including a transistor.

40. The computer-readable medium of claim 28, wherein the integrated optical/electronic circuit is at least partially formed on a Silicon-On-Insulator (SOI) substrate.

41. The computer-readable medium of claim 40, wherein the optical design portion partially models a waveguide included in said at least certain optical circuits.

42. The computer-readable medium of claim 41, wherein said SOI substrate includes a substrate layer, and wherein said waveguide at least partially extends within said substrate layer.

43. The computer readable medium of claim 28, wherein the processor models the operation of one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

44. A method of operating a computer processor, the computer processor using computer software, the computer software is configured to simulate the electrical characteristics and the optical characteristics of an integrated optical/electronic circuit, the method comprising:

generating topology information and free-carrier concentration information by simulating operation of at least certain electronics circuits of said integrated optical/electronic circuit using an electronic design portion; and

simulating operation of at least certain optical circuits of said integrated optical/electronic

circuit in an optical design portion in response to said topology information and said free-carrier concentration information generated by said electronic design portion.

45. The method of claim 44, wherein the electronic design portion includes a process simulation portion that generates said topology information.

46. The method of claim 44, wherein the electronic design portion includes a device simulation portion that generates said free-carrier concentration information.

47. The method of claim 44, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion.

48. The method of claim 44, wherein said optical design portion further comprises at least one of the group consisting of: a waveguide grating portion, a diffraction optical element portion, a finite difference time domain portion, a thin film portion, a beam propagation method portion, and a raytracing portion.

49. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including one from the group of a focusing mirror, a waveguide, and a Fabry-Perot cavity.

50. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a wavelength division multiplexer modulator.

51. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including an evanescent coupler.

52. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a diode.

53. The method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a transistor.

54. The method of claim 44, wherein the integrated optical/electronic circuit is at least partially formed on a Silicon-On-Insulator (SOI) substrate.

55. The method of claim 54, wherein the optical simulation design tools portion partially models a waveguide included in said at least certain optical circuits.

56. The method of claim 55, wherein said SOI substrate includes a substrate layer, and

wherein said waveguide at least partially extends within said substrate layer.

57. The method of claim 44, wherein the computer processor modeling computer software simulates one from the group of a p-n device, a field plated device, a Schottky device, a MOSCAP, and a MOSFET.

IN THE DRAWINGS

Applicant respectfully requests the Examiner's approval of the proposed changes to the drawing figures 5, 13, 20, 21, 22, 30, 47, 51, 52, 59, 60, 68A, 68B, 68C, 68D, 73, 74, 75, 76, 77, 78, 82, 83 and 88 in the request for Approval of Drawing Changes filed concurrently herewith.

IN THE SPECIFICATION

Rewrite the title on page 1, that starts on line 1 and ends on line 2 to read as follows.

SIMULATION PROGRAM FOR INTEGRATED OPTICAL/ELECTRONIC CIRCUIT

Rewrite the paragraph on page 1, that starts on line 5 and ends on line 6 to read as follows.

This application is a divisional of U.S. Patent Application Serial No. 09/991,542, filed November 10, 2001, which is a continuation-in-part of U.S. Patent Application Serial No. 09/859,693, filed May 17, 2001. U.S. Patent Application Serial No. 09/991,542 claims priority to U.S. Provisional Application No. 60/293,615, filed May 25, 2001 and U.S. Provisional Application No. 60/297,208, filed June 8, 2001.

Please delete the paragraph on page 1, that starts on line 7 and ends on line 8.

Please delete the paragraph on page 1, that starts on line 9 and ends on line 10.

Rewrite the paragraph on page 4, that starts on line 17 and ends on line 22 to read as follows.

FIGs. 15A to 15D show side cross section views of the optical waveguide device of FIG. 13 or taken through sectional lines 15-15 in FIG. 13, FIG. 15A shows both gate electrodes 1304,

1306 being deactivated, FIG. 15B shows the gate electrode 1304 being actuated as the gate electrode 1306 is deactivated, FIG. 15C shows the gate electrode 1304 being deactuated as the gate electrode 1306 is activated, and FIG. 15D shows both gate electrodes 1304 and 1306 being actuated;

Rewrite the paragraph on page 9, that starts on line 7 and ends on line 8 to read as follows.

FIGs. 63A to 63D show a method of fabricating the partially completed integrated optical/electronic circuit of FIG. 51;

Rewrite the paragraph on page 9, that starts on line 9 and ends on line 10 to read as follows.

FIG. 64 shows a plot of intensity versus distance from a ledge of one embodiment of input/output light coupler 112 including a tapered gap portion;

Rewrite the paragraph on page 9, that starts on line 11 and ends on line 12 to read as follows.

FIG. 65 shows another plot of intensity at a prism base for another embodiment of input/output light coupler having a prism, but without a tapered gap portion;

Please delete the paragraph on page 9, that starts on line 13 and ends on line 14.

Rewrite the paragraph on page 9, that starts on line 15 and ends on line 16 to read as follows.

FIG. 66 shows one embodiment of hybrid active electronic and optical circuit that is configured as a J-coupler;

Please delete the paragraph on page 9, that starts on line 17 and ends on line 18.

Rewrite the paragraph on page 9, that starts on line 21 and ends on line 21 to read as follows.

FIGs. 68A to 68D show one embodiment of a method of anisotropically etching using a mask.

Rewrite the paragraph on page 12, that starts on line 16 and ends on line 19 to read as follows.

Actual embodiments of discrete optical waveguide devices are described in the "Specific Embodiments of Optical Waveguide Device" portions of this disclosure. More complex optical circuits including a plurality of optical waveguide devices 100 are described in the "Optical Circuits Including Optical Waveguide Devices" portion of this disclosure.

Rewrite the paragraph on page 13, that starts on line 16 and ends on line 25 to read as follows.

FIGs. 51 to 52 show one embodiment of an integrated optical/electric circuit 103. Multiple embodiments of integrated optical/electric circuit 103 are described herein as being formed using SOI devices, etc. The integrated optical/electric circuit can be configured with and combination of active optical, passive optical, active electronics, and passive components circuit. SOI technology is highly promising for integrated optical/electronic circuits, and using relatively thin SOI devices (having an upper silicon layer less than 10 μ) has many benefits. Using thin SOI devices for waveguides limits the vertical locations in which light can diffract, and therefor acts to localize the light to a relatively narrow waveguide. Thin SOI devices can be formed using planar lithography techniques including deposition and etching processes.

Rewrite the paragraph that starts on page 16, line 10 and continues over to page 17, line 1 to read as follows.

The embodiments of optical waveguide device 100 shown in multiple figures including FIGs. 1-3, and 5, etc. include a field effect transistor (FET) portion 116 that is electrically coupled to a waveguide 106. One embodiment of the waveguide is fabricated proximate to, and underneath, the gate electrode of the FET portion 116. The waveguide 106 is typically made from silicon or another one or plurality of III-V semiconductors. The FET portion 116 includes a first body contact electrode 118, a gate electrode 120, and a second body contact electrode 122.

A voltage can be applied by e.g., a voltage source 202 to one of the electrodes. The gate electrode 120 is the most common electrode in which the voltage level is varied to control the optical waveguide device. If the first body contact portion 118 and the second body contact portion are held at the same voltage by placing an electrical connector 204 there between, then the optical waveguide device 100 operates as a diode. If there is not an electrical connector between the first body contact portion 118 and the second body contact portion 122, then the optical waveguide device 100 acts as a transistor. This is true for each of the following FET/diode configurations. Whether any FET optical waveguide device 100 is biased to act as a transistor or diode, the optical waveguide device 100 is within the intended scope of the present invention since either a diode or a transistor is capable of altering the effective mode index in the waveguide as described herein.

Rewrite the paragraph on page 67, that starts on line 9 and ends on line 24 to read as follows.

FIG. 30 shows another embodiment of an optical waveguide device 100 including a grating 3008 that is used as a lens to focus light passing through the waveguide. The embodiment of optical waveguide device 100, or more particularly the FIG. 2 embodiment of gate electrode of the optical waveguide device, is modified by replacing the continuous gate electrode (in FIG. 2) with a discontinuous electrode in the shape of a grating (shown in FIG. 30). The grating 3008 is formed with a plurality of etchings 3010 that each substantially parallels the optical path 101 of the optical waveguide device. In the FIG. 30 embodiment of grating 3008, the thickness of the successive etchings 3010 to collectively form gate electrode 120 increases

toward the center of the optical waveguide device, and decreases toward the edges 120a, 120b of the gate electrode 120. Therefore, the region of changeable propagation constant 190 in the waveguide is thicker at those regions near the center of the waveguide. Conversely, the region of changeable propagation constant 190 becomes progressively thinner at those regions of the waveguide near edges 120a, 120b. The propagation constant is a factor of both the volume and the shape of the material used to form the gate electrode. The propagation constant is thus higher for those regions of changeable propagation constant closer to the center of the waveguide.

Rewrite the paragraph that starts on page 84, line 24 and continues over to page 85, line 10 to read as follows.

The high propagation constant bands 4502 correspond to the location of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The low propagation constant bands 4504 correspond to the bands between the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The high propagation constant bands 4502 and the low propagation constant bands 4504 extend vertically through the waveguide. The input mirror gate electrodes 4402 and the output mirror gate electrodes 4404 can be shaped to provide, e.g., a concave mirror surface if desired. Additionally, deactuation of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404 removes any effect of the high propagation constant bands 4502 and low propagation constant bands 4504 from the waveguide of the resonator 4400. Such effects are removed since the propagation constant approaches a uniform level corresponding to 0 volts applied to the gate electrodes 4402, 4404.

Rewrite the paragraph on page 89, that starts on line 17 and ends on line 23 to read as follows.

The wavelength separator 3902 acts to filter or modulate the wavelength of an incoming signal over waveguide 3916 into a plurality of light signals. Each of these light signals has a different frequency. Each of a plurality of waveguides 3918a to 3918d contain a light signal of different wavelength λ_1 to λ_n, the wavelength of each signal corresponds to a prescribed limited bandwidth. For example, waveguide 3918a carries light having a color corresponding to wavelength λ_1, while waveguide 3918b carries a light having a color corresponding to wavelength λ_2, etc.

Rewrite the heading on page 100, line 12 to read as follows.

VI. Generalization of Active Optical Devices in SOI

Rewrite the heading on page 101, line 4 to read as follows.

VII. INPUT/OUTPUT COUPLING EMBODIMENTS

Rewrite the paragraph on page 105, that starts on line 5 and ends on line 19 to read as follows.

It is envisioned that the levels of silicon layers of the on-chip electronics portion 5101 are formed simultaneously with the one or more layers of the evanescent coupling region 5106, (or the gap portion), and/or the light coupling portion 5110 of the input/output light coupler 112. In other words, any pair of vertically separated layers on the on-chip electronics portion 5101 may be formed simultaneously with any portion of optical elements 5106, 5110 that is at substantially the same vertical level using, for example, planar lithography or projection lithography techniques. Therefore, any one of the one or more layers of the evanescent coupling region 5106 and/or the light coupling portion 5110 that are at generally the same vertical height as the layers on the electronics portion 5101 will be formed simultaneously, although the different portions will undergo different doping, masking, ion implantation, or other processes to provide the desired optical and/or electronic characteristics. As such, technology, know how, processing time, and equipment that has been developed relative to the fabrication of electronic circuits (e.g., techniques for fabricating thin SOI semiconductor chips) can be used to construct optical and electronic circuits simultaneously on the same substrate.

Rewrite the paragraph on page 108, that starts on line 11 and ends on line 23 to read as follows.

The embodiment of input/output light coupler 112 shown in FIG. 55 includes a ledge 5502 that forms a support base for one edge of the light coupling portion 5110 (e.g., a prism or grating). The ledge 5502 may have thickness that provides the desired angle of the base of the input/output light coupler 112. The ledge 5502 is preferably formed by removing sacrificial material at the optical I/O location using an etching process, and the base of the light coupling

portion 5110 is angled at a slight angle by resting it on the ledge 5502. In certain embodiments, the height of the ledge 5502 is in the range of under fifty microns, and may actually be in the range of one or a couple of microns. The gap portion 5106 may be filled with such optically clear polymer or glass material that provides the desired optical characteristics to the light entering into, or exiting from, the waveguide. Light rays 5120 passing through the embodiment of input/output light coupler 112, shown in the embodiment of FIG. 55, must satisfy the basic principles described relative to FIG. 51, e.g., equation 23.

Rewrite the paragraph on page 112, that starts on line 8 and ends on line 24 to read as follows.

As light is exiting the output coupler from the waveguide, wherein the waveguide is carrying substantially uniform intensity of light across the cross-sectional area of the waveguide, it may be desired to once again convert the light exiting the output coupler into a light beam that has a Gaussian intensity profile. Evanescent couplings configured as a tapered gap portion 5106 as illustrated particularly in FIGS. 55 and 57, result in a closer fit to a Gaussian profile than without the taper gap portion. For example, FIG. 64 shows the calculations for a 0.2 micron silicon waveguide formed with the taper. The tapered gap portion is illustrated by line 6402 in FIG. 64, and the height of the taper from the waveguide is illustrated along the right ordinate of FIG. 64. An intensity profile curve 6406 is plotted to indicate the intensity profile at the base of the input/output light coupling device. The relative intensity value is plotted as the left ordinate in FIG. 64. The abscissa measures the distance from a ledge (an arbitrary measuring point) in microns. A best fit Gaussian curve 6404 is plotted proximate the intensity profile 6406, to

illustrate how effectively the output light from the output coupler models the Gaussian curve. FIG. 65 shows a similar curve as FIG. 64, except FIG. 65 models a constant thickness gap, as indicated by the fact that the taper curve 6410 is level in FIG. 65. Curve 6412 of FIG. 65 measures the intensity profile for an output beam of light that is not Gaussian, but instead exponential.

Rewrite the paragraph that starts on page 119, line 18 and continues over to page 120, line 6 to read as follows.

FIGS. 63A to 63D, show a process of simultaneously depositing silica, other suitable dielectric, polysilicon, etc. layer on both the light coupling portion 5110 and the electronic portion 5101. Initially, a silicon layer 6302 is deposited somewhat uniformly across the entire integrated optical/electrical circuit 103, including both the electronics portion 5101 and the light coupling portion 5110. Both the embodiments of the light coupling portion that may include prisms, as well as gratings, rely upon homogenous build up of silica throughout the entire light coupling portion. By comparison, the electronics portion 5101 is formed using a series of silica layers, interspersed with metallic interconnects through which metallic vias vertically extend. Therefore, a series of additional metalization and other steps are necessary between successive depositions of silica. By comparison, since the light coupling portion is homogenous, relatively little processing will occur between the various silica deposition steps. In FIG. 63A, the layer of silicon 6302 is deposited on the upper surface of the integrated optical/electrical circuit 103 using known silicon deposition techniques, such as chemical vapor deposition and sputtering.

Rewrite the paragraph on page 120, that starts on line 7 and ends on line 15 to read as follows.

The planer lithography method continues in FIG. 63B in which a photoresist layer 6304 is deposited on the upper surface of the deposited silicon layer 6302. Photoresist may be applied, and then the substrate 102 typically spun so that the photoresist layer is extended under the influence of centrifugal force to a substantially uniform thickness. In FIG. 63C, the lithography portion 6308 selectively applies light to the upper surface of the photoresist layer 6304, thereby acting to develop certain regions of the photoresist layer. Depending upon the type of photoresist, the photoresist may harden either if light is applied to it, or will not harden if light is not applied. The lithography portion 6308 includes a lithography light source 6310 and a lithography mask 6312.

Rewrite the paragraph that starts on page 120, line 23 and continues over to page 121, line 8 to read as follows.

The photoresist layer 6304 is then washed, in which the undeveloped portions of the photoresist are substantially washed away while the developed portions of the photoresist layer remain as deposited. The developed, and thereby remaining portions of the photoresist layer thereupon cover the silicon thereby allowing for selected portions of the silicon layer to be etched. The etching acts on those uncovered portions of the silicon layers 6302 that correspond to the undeveloped regions of the photoresist layer. During etching, the developed portions of the photoresist layer 6304 cover, and protect, the covered portions of the silicon layer 6302, and

protect the covered portions of the silicon layer 6302 from the etchant. Following the etching, respective structures 6350 and 6352 remain that are ultimately used to form part of the respective optical (e.g., the input/output light coupler 112) and electronic (e.g., electronic portion 5101) portions.

Rewrite the heading on page 122, line 1 to read as follows.

VIII. Hybrid Active Electronic and Optical Circuits

Rewrite the paragraph that starts on page 124, line 23 and continues over to page 125, line 3 to read as follows.

FIG. 68 shows a side view of the hybrid active electronic and optical circuit 6502 such as shown in FIG. 66, during processing. The hybrid active electronic and optical circuit 6502 is formed on top of an SOI wafer 6600. The SOI wafer 6600 is initially formed with a planar upper surface. A photoresist layer 6804 is initially applied to the upper surface of the SOI wafer 6600. A photolithography mask is applied to the upper surface of the SOI wafer 6600 and the light is applied to the photolithography mask.

Rewrite the paragraph on page 125, that starts on line 4 and ends on line 9 to read as follows.

The purpose of the etching process using photolithography is to remove necessary portions of the upper most silicon layer in order to provide function of the passive optical component 6506, the active electronics portion 6504, the other electronic components 6602, and the other optical components 6604. The shape of the active electronic portion 6504, the other electronic components 6602, and the other optical components 6604 are shown in FIG. 66.

Rewrite the paragraph that starts on page 130, line 21 and continues over to page 131, line 3 to read as follows.

FIG. 70 shows another embodiment of hybrid active electronic and optical circuit 6502 as shown in FIG. 69, except that the waveguide prism 7002 has been incorporated in place of the waveguide grating 6902. Similarly, the waveguide prism 7002 is a passive device, that deflects the light being applied to the waveguide 6904 in a mode angle θ_M. The use of the active electronic component 6504 allows adjustability of the light flowing through the waveguide prism 7002, thereby allowing light flowing through the waveguide prism 7002 to be controllably directed at a desired controllable angle to the waveguide 6904.

Rewrite the paragraph on page 132, that starts on line 7 and ends on line 15 to read as follows.

The Fabry-Perot cavity 7302 as shown in FIG. 73 represents another hybrid active electronic and optical circuit that may be formed on the silicon layer or an SOI wafer, and includes a plurality of passive optical portions 6506 and an active opto-electronic portion 6504.

The passive optical portion 6506 includes a waveguide 7310 and a plurality of gratings 7312. The gratings 7312 may be configured in a similar manner as Bragg gratings, surface gratings, or other known types of gratings. This Fabry-Perot waveguide operates similar to the well understood Fabry-Perot cavities used in optics. The reflectivity of mirrors (in this embodiment, the gratings act as mirrors) and the cavity optical length determine the reflection/transmission profile of the device.

Rewrite the paragraph that starts on page 133, line 22 and continues over to page 134, line 4 to read as follows.

The embodiment of grating 7304 shown in FIG. 75 is a passive device. In the Fabry-Perot cavity 7302 and the coupled Fabry-Perot cavity 7402 shown respectively in FIGS. 73 and 74, the respective active opto-electric portion 6504 is positioned between adjacent gratings 7304. It may be desired to provide a grating structure that is an active device. As such, the wavelengths of light that each grating could reflect or deflect could be controlled. FIGS. 77 and 76 show two alternate embodiments of active gratings 7602. The embodiments of gratings 7602 shown in FIGS. 76 and 77 thus are configured as hybrid active electronic and optical circuits 6502.

Rewrite the paragraph on page 135, that starts on line 1 and ends on line 13 to read as follows.

The upper silicon layer 6601 can be built up to the height equal to the raised lands 7502. Following this uniform build up of the upper silicon layer 6601, a uniform metalization layer can be applied across the entire upper surface of the upper silicon layer. At this time, the upper silicon layer will be thickened by the addition of silicon, and coated by a metal layer corresponding to the active electronic portion 6504. Those portions of the upper layers 6601 that do not correspond to the raised lands 7502 can have the upper middle layer etched away using known metal etching techniques. Following the etching away of the middle layer, the region of the upper silicon layers 6601 that are not coated by the remaining portions of the etched metal, i.e., the silicon areas corresponding to the lowered lands 7504, can be etched away using known silicon etching techniques. The etching of both the metal areas and the silicon layers utilizes masks that have openings, the regions of the openings corresponding either to the areas that are going to be etched or the areas that are not going to be etched.

Rewrite the paragraph on page 135, that starts on line 14 and ends on line 20 to read as follows.

In those embodiments of gratings 7602 in which silicon material 7620 is not added to the original upper silicon layer 6601, a metalized layer is added to the upper surface of the upper silicon layer 6601. The depth of the metal layer corresponds to the desired depth of the active electronic portion 6504. The techniques of etching away the metal layer of the active electronic portion 6504 and the underlying sacrificial silicon material of the upper silicon layer 6601 are similar to that described with respect to the removal of the metal and silicon portions where silicon has been added.

Rewrite the paragraph that starts on page 135, line 21 and continues over to page 136, line 3 to read as follows.

To fabricate the embodiment of the grating 7602 shown in FIG. 77, the entire upper silicon layer 6601 is built up to the desired height of the raised lands 7502. If the upper silicon layers are higher than the desired height of the raised lands 7502, then the entire upper silicon layer is etched uniformly down to the level of the raised lands 7502. Following the etching or metal deposition, it may be necessary to level the upper surface of the upper silicon layers using such means as, e.g., a chemical, mechanical polisher (CMP). Following the CMP processing, a photoresist is added to the upper surface of the upper silicon layer 6601.

Rewrite the paragraph on page 136, that starts on line 4 and ends on line 13 to read as follows.

Masks are used to define which area, depending upon the type of photoresist, are going to be etched away and light is applied through the apertures in the masks to the upper surface of the upper silicon layer 6601 to develop the photoresist, if necessary, to define which regions will be etched. Etching is then performed on the uncovered portions of the upper surface of the upper silicon layer 6601, until those uncovered portions are lowered to the level to the lower lands 7504. The upper surface of the lower lands 7504 are then coated with the metal layer corresponding to the active electronic portion 6504 of the grating. The deposition of the metal on the upper surface of the lower lands 7504 can be performed using a mask whose opening

corresponds to the regions of the upper silicon layers 6601 that have been etched down to the lower lands 7504.

Rewrite the paragraph on page 137, that starts on line 11 and ends on line 20.

FIG. 78 shows two gratings of the active chirped gratings regions 7806 being actuated, thereby diverting optical signals having wavelengths λ_1 and λ_5 to the passive chirped grating region 7814. Light having different wavelengths can thus be used to contain distinct data transmitted as optical signals. Data signals from the data electronic input portion 7816 may be applied to control the individual components of the active chirped grating region 7806. The data electronic input portion 7816 can be fabricated at the same time, on the chip, as the active electronic portions 6504 and the passive optical portion 6502 shown in the embodiments of FIGS. 76, 77 and 75 respectively. As such, the embodiment of wavelength division multiplexer modulator 7802 shown in FIG. 78 can be considered as an embodiment of hybrid active electronic and optical circuit 7602.

Rewrite the heading on page 141, line 4 to read as follows.

IX. Photonic Band Gap Device

Rewrite the paragraph on page 145, that starts on line 9 and ends on line 20 to read as follows.

FIG. 83 shows one embodiment of passive photonic band gap device (referred to as a shallow passive photonic band gap device 9010) whose region of photonic crystals is delineated by shallow pillars which do not extend through the entire vertical height of the waveguide. In one embodiment, the shallow passive pillars extend from the upper surface for a height h, but do not extend fully through the waveguide. Each one of the shallow passive pillars 9220 can be biased to control the relative dielectric constants of those areas of waveguide material set forth under the shallow passive pillars. In certain embodiments of shallow passive photonic band gap devices, the pillars are formed as wells, recesses, or indentations in the upper surface of the waveguide. FIG. 85 shows a top view of one embodiment of circular recesses that define the shape of the pillars. The pillars can also be defined by the square, rectangular, or some other regularly repeated shape, as opposed to circular holes.

Rewrite the heading on page 151, line 6 to read as follows.

X. Simulation Program For Hybrid Active Electronic and Optical Circuits

REMARKS

Claims 12-57 are pending in the application. Claims 1-11 have been canceled. Claims 12-57 are newly added.

The present Preliminary Amendment seeks to correct several typographical errors in the specification discovered after filing of the parent application. It is respectfully submitted that no new matter has been introduced as a result of the amendments made herein.

In addition, applicant notes that there was an erroneous reference to Application Serial No. 09/859,593, in the domestic priority claim listed on page 1 of the parent application. In particular, applicant notes that the parent application, among other things, claims domestic priority to Application Serial No. 09/859,693, filed May 17, 2001. Applicant notes that the attached Declaration and Power of Attorney form correctly refers to Application Serial No. 09/859,693, filed May 17, 2001, in its priority claim; and a corresponding correction was previously made in the parent application. In addition, applicant notes that the attached Preliminary Amendment has modified the priority claim at page 1, line 6 of the application, so as to correctly refer to Application Serial No. 09/859,693 filed May 17, 2001.

An early and favorable office action is earnestly solicited.

The Commissioner is hereby authorized to charge any deficiency in the enclosed amount or credit any overpayment to Deposit Account No. 50-0310.

Respectfully submitted,

Daniel H. Golub
Registration No. 33,701

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1701 Market Street
Philadelphia, PA 19103-2921
215.963.5055

Dated: February 15, 2002

SPECIFICATION WITH MARKINGS TO SHOW CHANGES MADE

The title on page 1, that starts on line 1 and ends on line 2.

SIMULATION PROGRAM FOR INTEGRATED OPTICAL/ELECTRONIC CIRCUIT

[INTEGRATED OPTICAL/ELECTRONIC CIRCUITS AND ASSOCIATED METHODS OF SIMULTANEOUS GENERATION THEREOF]

The paragraph on page 1, that starts on line 5 and ends on line 6.

This application is a continuation-in-part to U.S. Patent Application Serial No. 09/859,693 [09/859,593], filed May 17, 2001.

The paragraph on page 4, that starts on line 17 and ends on line 22.

[FIG. 15, including]FIGs. 15A to 15D[,] show side cross section views of the optical waveguide device of FIG. 13 or taken through sectional lines 15-15 in FIG. 13, FIG. 15A shows both gate electrodes 1304, 1306 being deactivated, FIG. 15B shows the gate electrode 1304 being actuated as the gate electrode 1306 is deactivated, FIG. 15C shows the gate electrode 1304 being deactuated as the gate electrode 1306 is activated, and FIG. 15D shows both gate electrodes 1304 and 1306 being actuated;

The paragraph on page 9, that starts on line 7 and ends on line 8.

[FIG. 63, including] FIGs. 63A to 63D[,] show[s] a method of fabricating the partially completed integrated optical/electronic circuit of FIG. 51;

The paragraph on page 9, that starts on line 9 and ends on line 10.

FIG. 64 [64A] shows a plot of intensity versus distance from a ledge of one embodiment of input/output light coupler 112 including a tapered gap portion;

The paragraph on page 9, that starts on line 11 and ends on line 12.

FIG. 65 [64B] shows another plot of intensity at a prism base for another embodiment of input/output light coupler having a prism, but without a tapered gap portion;

The paragraph on page 9, that starts on line 13 and ends on line 14.

[FIG. 64 shows the integrated optical/electronic circuit of FIG. 51 during a portion of the processing;]

The paragraph on page 9, that starts on line 15 and ends on line 16.

FIG. 66 [65] shows [a perspective view of] one embodiment of hybrid active electronic and optical circuit that is configured as a J-coupler;

The paragraph on page 9, that starts on line 17 and ends on line 18.

[FIG. 66 shows a top view of the hybrid active electronic and optical circuit of FIG. 65;]

The paragraph on page 9, that starts on line 21 and ends on line 21.

FIGs. 68A to 68D [FIG. 68] show[s] one embodiment of a method of anisotropically etching using a mask.

The paragraph on page 12, that starts on line 16 and ends on line 19.

Actual embodiments of discrete optical waveguide devices are described in the "Specific Embodiments of Optical Waveguide Device" portions of this disclosure. More complex optical circuits including a plurality of optical waveguide devices 100 [103] are described in the "Optical Circuits Including Optical Waveguide Devices" portion of this disclosure.

The paragraph on page 13, that starts on line 16 and ends on line 25.

FIGs. 51 to 52 [FIG. 1] show[s] one embodiment of an integrated optical/electric circuit 103. Multiple embodiments of integrated optical/electric circuit 103 are described herein as being formed using SOI devices, etc. The integrated optical/electric circuit can be configured with and combination of active optical, passive optical, active electronics, and passive components circuit. SOI technology is highly promising for integrated optical/electronic

circuits, and using relatively thin SOI devices (having an upper silicon layer less than 10 μ) has many benefits. Using thin SOI devices for waveguides limits the vertical locations in which light can diffract, and therefor acts to localize the light to a relatively narrow waveguide. Thin SOI devices can be formed using planar lithography techniques including deposition and etching processes.

The paragraph that starts on page 16, line 10 and continues over to page 17, line 1.

The embodiments of optical waveguide device 100 shown in multiple figures including FIGs. 1-3, and 5, etc. include a field effect transistor (FET) portion 116 that is electrically coupled to a waveguide 106. One embodiment of the waveguide is fabricated proximate to, and underneath, the gate electrode of the FET portion 116. The waveguide 106 is typically made from silicon or another one or plurality of III-V semiconductors. The FET portion 116 includes a first body contact electrode 118, a gate electrode 120, and a second body contact electrode 122. A voltage can be applied by e.g., a voltage source 202 to one of the electrodes. The gate electrode 120 is the most common electrode in which the voltage level is varied to control the optical waveguide device. If the first body contact portion 118 and the second body contact portion are held at the same voltage by placing an electrical connector 204 there between, then the optical waveguide device 100 operates as a diode. If there is not an electrical connector between the first body contact portion 118 and the second body contact portion 122, then the optical waveguide device 100 acts as a transistor. This is true for each of the following FET/diode configurations. Whether any FET optical waveguide device 100 is biased to act as a transistor or diode, the optical waveguide device 100 is within the intended scope of the present

invention since either a diode or a transistor is capable of altering the effective mode index in the waveguide as described herein.

The paragraph on page 67, that starts on line 9 and ends on line 24.

FIG. 30 shows another embodiment of an optical waveguide device 100 including a grating 3008 that is used as a lens to focus light passing through the waveguide. The embodiment of optical waveguide device 100, or more particularly the FIG. 2 embodiment of gate electrode of the optical waveguide device, is modified by replacing the continuous gate electrode (in FIG. 2) with a discontinuous electrode in the shape of a grating (shown in FIG. 30). The grating 3008 is formed with a plurality of etchings 3010 that each substantially parallels the optical path 101 of the optical waveguide device. In the FIG. 30 embodiment of grating 3008, the thickness of the successive etchings 3010 to collectively form gate electrode 120 increases toward the center of the optical waveguide device, and decreases toward the edges 120a, 120b of the gate electrode 120. Therefore, the region of changeable propagation constant 190 in the waveguide is thicker at those regions near the center of the waveguide. Conversely, the region of changeable propagation constant 190 becomes progressively thinner at those regions of the waveguide near edges 120a, 120b. The propagation constant is a factor of both the volume and the shape of the material used to form the gate electrode. The propagation constant is thus higher for those regions of changeable propagation constant closer to the center of the waveguide.

The paragraph that starts on page 84, line 24 and continues over to page 85, line 10.

The high propagation constant bands 4502 correspond to the location of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The low propagation constant bands 4504 correspond to the bands between the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404. The high propagation constant bands 4502 and the low propagation constant bands 4504 extend vertically through the waveguide. The input mirror gate electrodes 4402 and the output mirror gate electrodes 4404 can be shaped to provide, e.g., a concave mirror surface if desired. Additionally, deactuation of the input mirror gate electrodes 4402 or the output mirror gate electrodes 4404 removes any effect of the high propagation constant bands 4502 and low propagation constant bands 4504 from the waveguide of the resonator 4400. Such effects are removed since the propagation constant approaches a uniform level corresponding to 0 volts applied to the gate electrodes 4402, 4404 [4502, 4504].

The paragraph on page 89, that starts on line 17 and ends on line 23.

The wavelength separator 3902 acts to filter or modulate the wavelength of an incoming signal over waveguide 3916 into a plurality of light signals. Each of these light signals has a different frequency. Each of a plurality of waveguides 3918a to 3918d contain a light signal of different wavelength λ_1 to λ_n, the wavelength of each signal corresponds to a prescribed limited bandwidth. For example, waveguide 3918a carries light having a color corresponding to wavelength λ_1, while waveguide 3918b carries a light having a color corresponding to wavelength λ_2, etc.

The heading on page 100, line 12.

VI. [A] Generalization of Active Optical Devices in SOI

The heading on page 101, line 4.

VII. INPUT/OUTPUT COUPLING EMBODIMENTS

The paragraph on page 105, that starts on line 5 and ends on line 19.

It is envisioned that the levels of silicon layers of the on-chip electronics portion 5101 are formed simultaneously with the one or more layers of the evanescent coupling region 5106, (or the gap portion), and/or the light coupling portion 5110 of the input/output light coupler 112. In other words, any pair of vertically separated layers on the on-chip electronics portion 5101 may be formed simultaneously with any portion of optical elements 5106,[5108,] 5110 that is at substantially the same vertical level using, for example, planar lithography or projection lithography techniques. Therefore, any one of the one or more layers of the evanescent coupling region 5106 and/or the light coupling portion 5110 that are at generally the same vertical height as the layers on the electronics portion 5101 will be formed simultaneously, although the different portions will undergo different doping, masking, ion implantation, or other processes to provide the desired optical and/or electronic characteristics. As such, technology, know how, processing time, and equipment that has been developed relative to the fabrication of electronic circuits (e.g., techniques for fabricating thin SOI semiconductor chips) can be used to construct optical and electronic circuits simultaneously on the same substrate.

The paragraph on page 108, that starts on line 11 and ends on line 23.

The embodiment of input/output light coupler 112 shown in FIG. 55 includes a ledge 5502 that forms a support base for one edge of the light coupling portion 5110 (e.g., a prism or grating). The ledge 5502 may have thickness that provides the desired angle of the base of the [t he] input/output light coupler 112. The ledge 5502 is preferably formed by removing sacrificial material at the optical I/O location using an etching process, and the base of the light coupling portion 5110 is angled at a slight angle by resting it on the ledge 5502. In certain embodiments, the height of the ledge 5502 is in the range of under fifty microns, and may actually be in the range of one or a couple of microns. The gap portion 5106 may be filled with such optically clear polymer or glass material that provides the desired optical characteristics to the light entering into, or exiting from, the waveguide. Light rays 5120 passing through the embodiment of input/output light coupler 112, shown in the embodiment of FIG. 55, must satisfy the basic principles described relative to FIG. 51, e.g., equation 23.

The paragraph on page 112, that starts on line 8 and ends on line 24.

As light is exiting the output coupler from the waveguide, wherein the waveguide is carrying substantially uniform intensity of light across the cross-sectional area of the waveguide, it may be desired to once again convert the light exiting the output coupler into a light beam that has a Gaussian intensity profile. Evanescent couplings configured as a tapered gap portion 5106 as illustrated particularly in FIGS. 55 and 57, result in a closer fit to a Gaussian profile than

without the taper gap portion. For example, FIG. 64[A] shows the calculations for a 0.2 micron silicon waveguide formed with the taper. The tapered gap portion is illustrated by line 6402 in FIG. 64[A], and the height of the taper from the waveguide is illustrated along the right ordinate of FIG. 64[A]. An intensity profile curve 6406 is plotted to indicate the intensity profile at the base of the input/output light coupling device. The relative intensity value is plotted as the left ordinate in FIG. 64[A]. The abscissa measures the distance from a ledge (an arbitrary measuring point) in microns. A best fit Gaussian curve 6404 is plotted proximate the intensity profile 6406, to illustrate how effectively the output light from the output coupler models the Gaussian curve. FIG. 65 [64B] shows a similar curve as FIG. 64[A], except FIG. 65 [64B] models a constant thickness gap, as indicated by the fact that the taper curve 6410 is level in FIG. 65 [64B]. Curve 6412 of FIG. 65 measures the intensity profile for an output beam of light that is not Gaussian, but instead exponential.

The paragraph that starts on page 119, line 18 and continues over to page 120, line 6.

[FIG. 63, including]FIGS. 63A [a] to 63D [d], show a process of simultaneously depositing silica, other suitable dielectric, polysilicon, etc. layer on both the light coupling portion 5110 and the electronic portion 5101. Initially, a silicon layer 6302 is deposited somewhat uniformly across the entire integrated optical/electrical circuit 103, including both the electronics portion 5101 and the light coupling portion 5110. Both the embodiments of the light coupling portion that may include prisms, as well as gratings, rely upon homogenous build up of silica throughout the entire light coupling portion. By comparison, the electronics portion 5101 is formed using a series of silica layers, interspersed with metallic interconnects through which

metallic vias vertically extend. Therefore, a series of additional metalization and other steps are necessary between successive depositions of silica. By comparison, since the light coupling portion is homogenous, relatively little processing will occur between the various silica deposition steps. In FIG. 63A, the layer of silicon 6302 is deposited on the upper surface of the integrated optical/electrical circuit 103 using known silicon deposition techniques, such as chemical vapor deposition and sputtering.

The paragraph on page 120, that starts on line 7 and ends on line 15.

The planer lithography method continues in FIG. 63B [b] in which a photoresist layer 6304 is deposited on the upper surface of the deposited silicon layer 6302. Photoresist may be applied, and then the substrate 102 typically spun so that the photoresist layer is extended under the influence of centrifugal force to a substantially uniform thickness. In FIG. 63C, the lithography portion 6308 selectively applies light to the upper surface of the photoresist layer 6304, thereby acting to develop certain regions of the photoresist layer. Depending upon the type of photoresist, the photoresist may harden either if light is applied to it, or will not harden if light is not applied. The lithography portion 6308 includes a lithography light source 6310 and a lithography mask 6312.

The paragraph that starts on page 120, line 23 and continues over to page 121, line 8.

The photoresist layer 6304 is then washed, in which the undeveloped portions of the photoresist are substantially washed away while the developed portions of the photoresist layer

remain as deposited. The developed, and thereby remaining portions of the photoresist layer thereupon cover the silicon thereby allowing for selected portions of the silicon layer to be etched. The etching acts on those uncovered portions of the silicon layers 6302 that correspond to the undeveloped regions of the photoresist layer. During etching, the developed portions of the photoresist layer 6304 cover, and protect, the covered portions of the silicon layer 6302, and protect the covered portions of the silicon layer 6302 from the etchant. Following the etching, respective structures 6350 [6450] and 6352 [6452] remain that are ultimately used to form part of the respective optical (e.g., the input/output light coupler 112) and electronic (e.g., electronic portion 5101) portions.

The heading on page 122, that starts on line 1.

VIII. Hybrid Active Electronic and Optical Circuits

The paragraph that starts on page 124, line 23 and continues over to page 125, line 3.

FIG. 68 [66] shows a side [top] view of the hybrid active electronic and optical circuit 6502 such as shown in FIG. 66 [65], during processing. The hybrid active electronic and optical circuit 6502 is formed on top of an SOI wafer 6600. The SOI wafer 6600 is initially formed with a planar upper surface. A photoresist layer 6804 is initially applied to the upper surface of the SOI wafer 6600. A photolithography mask is applied to the upper surface of the SOI wafer 6600 and the light is applied to the photolithography mask.

The paragraph on page 125, that starts on line 4 and ends on line 9.

The purpose of the etching process using photolithography is to remove necessary portions of the upper most silicon layer in order to provide function of the passive optical component 6506, the active electronics portion 6504, the other electronic components 6602, and the other optical components 6604. The shape of the active electronic portion 6504, the other electronic components 6602, and the other optical components 6604 are shown in FIG. 66 [block].

The paragraph that starts on page 130, line 21 and continues over to page 131, line 3.

FIG. 70 shows another embodiment of hybrid active electronic and optical circuit 6502 as shown in FIG. 69, except that the waveguide prism 7002 has been incorporated in place of the waveguide grating 6902. Similarly, the waveguide prism 7002 is a passive device, that deflects the light being applied to the waveguide 6904 in a mode angle θ_M. The use of the active electronic component 6504 allows adjustability of the light flowing through the waveguide prism 7002, thereby allowing light flowing through the waveguide prism 7002 to be controllably directed at a desired controllable angle to the waveguide 6904.

The paragraph on page 132, that starts on line 7 and ends on line 15.

The Fabry-Perot cavity 7302 as shown in FIG. 73 represents another hybrid active electronic and optical circuit that may be formed on the silicon layer or an SOI wafer, and

includes a plurality of passive optical portions 6506 [7506] and an active opto-electronic portion 6504. The passive optical portion 6506 includes a waveguide 7310 and a plurality of gratings 7312. The gratings 7312 may be configured in a similar manner as Bragg gratings, surface gratings, or other known types of gratings. This Fabry-Perot waveguide operates similar to the well understood Fabry-Perot cavities used in optics. The reflectivity of mirrors (in this embodiment, the gratings act as mirrors) and the cavity optical length determine the reflection/transmission profile of the device.

The paragraph that starts on page 133, line 22 and continues over to page 134, line 4.

The embodiment of grating 7304 shown in FIG. 75 is a passive device. In the Fabry-Perot cavity 7302 and the coupled Fabry-Perot cavity 7402 shown respectively in FIGS. 73 and 74, the respective active opto-electric portion 6504 [6502] is positioned between adjacent gratings 7304. It may be desired to provide a grating structure that is an active device. As such, the wavelengths of light that each grating could reflect or deflect could be controlled. FIGS. 77 [75] and 76 show two alternate embodiments of active gratings 7602. The embodiments of gratings 7602 shown in FIGS. 76 and 77 thus are configured as hybrid active electronic and optical circuits 6502.

The paragraph on page 135, that starts on line 1 and ends on line 13.

The upper silicon layer 6601 can be built up to the height equal to the raised lands 7502. Following this uniform build up of the upper silicon layer 6601, a uniform metalization layer can

be applied across the entire upper surface of the upper silicon layer. At this time, the upper silicon layer will be thickened by the addition of silicon, and coated by a metal layer corresponding to the active electronic portion 6504. Those portions of the upper layers 6601 that do not correspond to the raised lands 7502 can have the upper middle layer etched away using known metal etching techniques. Following the etching away of the middle layer, the region of the upper silicon layers 6601 [7601] that are not coated by the remaining portions of the etched metal, i.e., the silicon areas corresponding to the lowered lands 7504, can be etched away using known silicon etching techniques. The etching of both the metal areas and the silicon layers utilizes masks that have openings, the regions of the openings corresponding either to the areas that are going to be etched or the areas that are not going to be etched.

The paragraph on page 135, that starts on line 14 and ends on line 20.

In those embodiments of gratings 7602 in which silicon material 7620 is not added to the original upper silicon layer 6601 [7601], a metalized layer is added to the upper surface of the upper silicon layer 6601 [7601]. The depth of the metal layer corresponds to the desired depth of the active electronic portion 6504. The techniques of etching away the metal layer of the active electronic portion 6504 and the underlying sacrificial silicon material of the upper silicon layer 6601 [7601] are similar to that described with respect to the removal of the metal and silicon portions where silicon has been added.

The paragraph that starts on page 135, line 21 and continues over to page 136, line 3.

To fabricate the embodiment of the grating 7602 shown in FIG. 77, the entire upper silicon layer 6601 [7601] is built up to the desired height of the raised lands 7502. If the upper silicon layers are higher than the desired height of the raised lands 7502, then the entire upper silicon layer is etched uniformly down to the level of the raised lands 7502. Following the etching or metal deposition, it may be necessary to level the upper surface of the upper silicon layers using such means as, e.g., a chemical, mechanical polisher (CMP). Following the CMP processing, a photoresist is added to the upper surface of the upper silicon layer 6601 [7601].

The paragraph on page 136, that starts on line 4 and ends on line 13.

Masks are used to define which area, depending upon the type of photoresist, are going to be etched away and light is applied through the apertures in the masks to the upper surface of the upper silicon layer 6601 [7601] to develop the photoresist, if necessary, to define which regions will be etched. Etching is then performed on the uncovered portions of the upper surface of the upper silicon layer 6601 [7601], until those uncovered portions are lowered to the level to the lower lands 7504. The upper surface of the lower lands 7504 are then coated with the metal layer corresponding to the active electronic portion 6504 of the grating. The deposition of the metal on the upper surface of the lower lands 7504 can be performed using a mask whose opening corresponds to the regions of the upper silicon layers 6601 [7601] that have been etched down to the lower lands 7504.

The paragraph on page 137, that starts on line 11 and ends on line 20.

FIG. 78 shows two gratings of the active chirped gratings regions 7806 being actuated, thereby diverting optical signals having wavelengths λ_1 and λ_5 to the passive chirped grating region 7814. Light having different wavelengths can thus be used to contain distinct data transmitted as optical signals. Data signals from the data electronic input portion 7816 may be applied to control the individual components of the active chirped grating region 7806. The data electronic input portion 7816 can be fabricated at the same time, on the chip, as the active electronic portions 6504 and the passive optical portion 6502 shown in the embodiments of FIGS. 76,[and]77 and 75 respectively. As such, the embodiment of wavelength division multiplexer modulator 7802 shown in FIG. 78 can be considered as an embodiment of hybrid active electronic and optical circuit 7602.

The heading on page 141, line 4.

IX. [IIIV.] Photonic Band Gap Device

The paragraph on page 145, that starts on line 9 and ends on line 20.

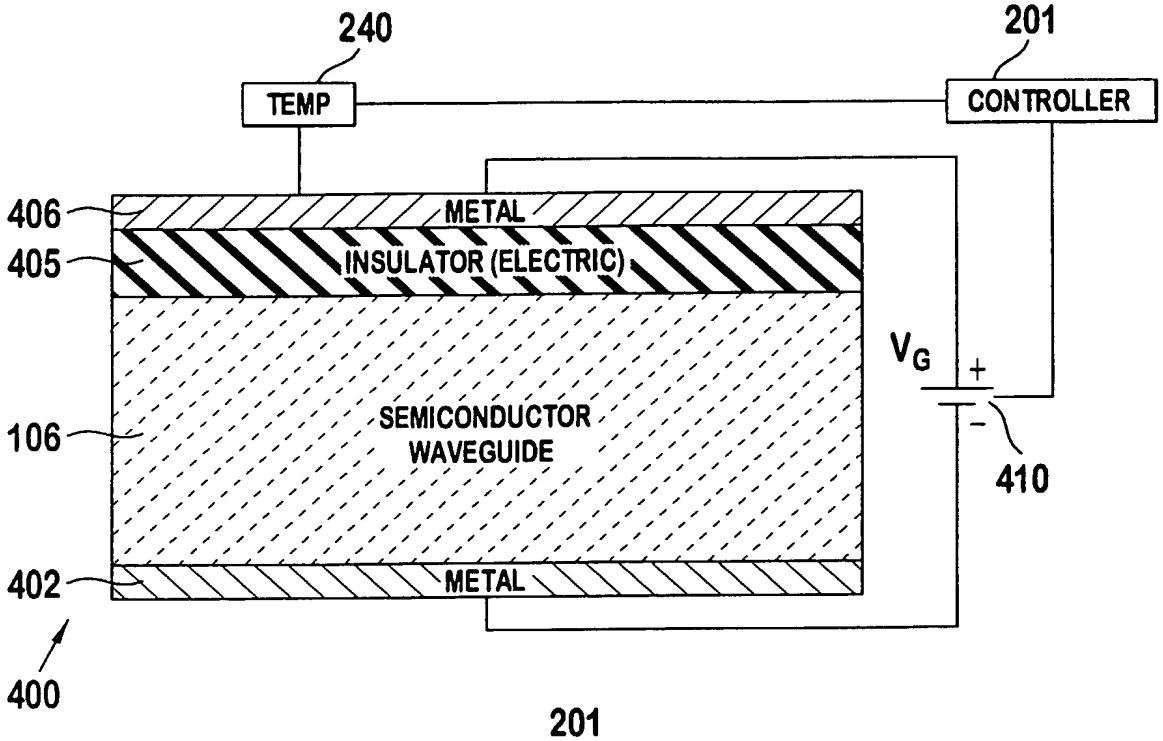
FIG. 83 shows one embodiment of passive photonic band gap device (referred to as a shallow passive photonic band gap device 9010) whose region of photonic crystals is delineated by shallow pillars which do not extend through the entire vertical height of the waveguide. In one embodiment, the shallow passive pillars extend from the upper surface for a height h, but do not extend fully through the waveguide. Each one of the shallow passive pillars 9220 can be biased to control the relative dielectric constants of those areas of waveguide material set forth

under the shallow passive pillars. In certain embodiments of shallow passive photonic band gap devices, the pillars are formed as wells, recesses, or indentations in the upper surface of the waveguide. FIG. 85 [87] shows a top view of one embodiment of circular recesses that define the shape of the pillars. The pillars can also be defined by the square, rectangular, or some other regularly repeated shape, as opposed to circular holes.

The heading on page 151, line 6.

X. [IX.] Simulation Program For Hybrid Active Electronic and Optical Circuits

FIG. 4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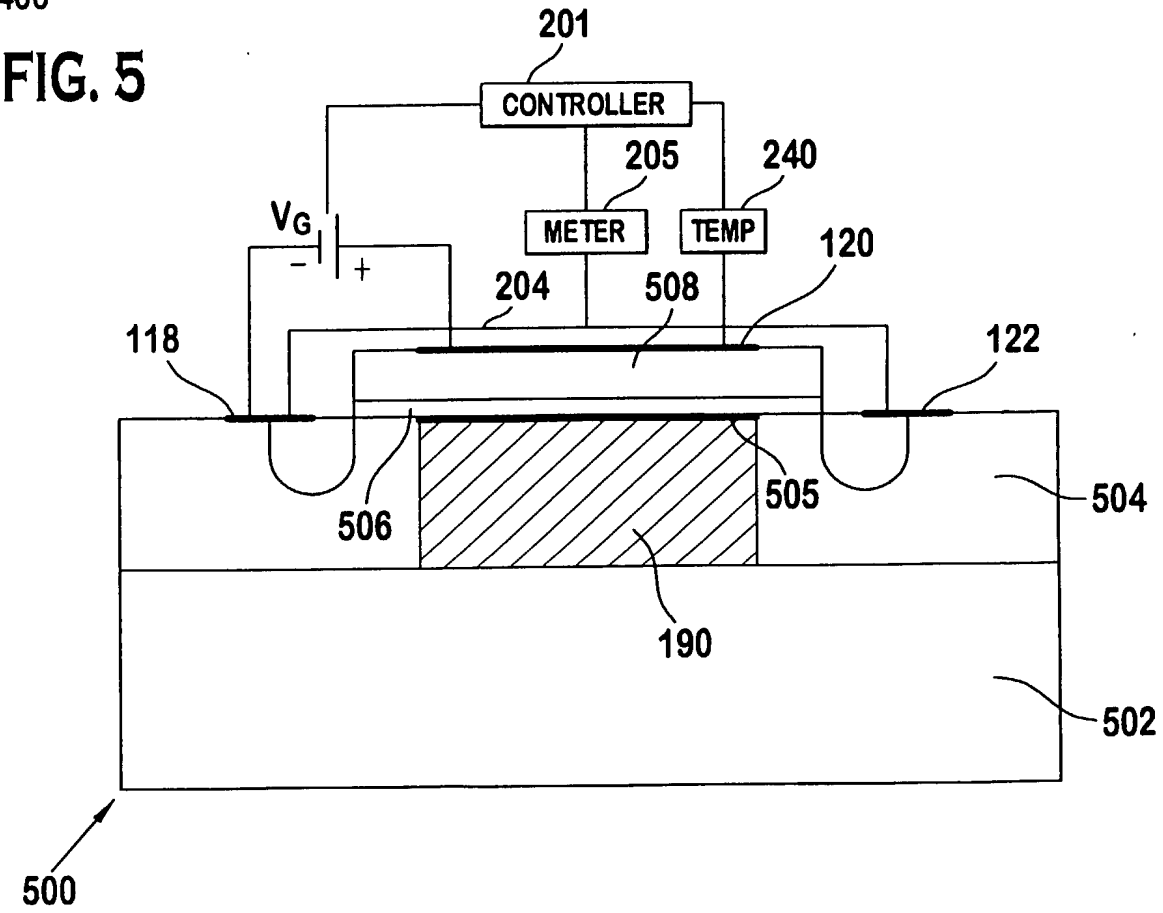
CONTROLLER
406
METAL
405
INSULATOR (ELECTRIC)
106
SEMICONDUCTOR
WAVEGUIDE
402
METAL
400
V_G
+
−
410

FIG. 5


201
CONTROLLER
205
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METER
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V_G
−
+
120
204
508
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505
504
190
502
500

FIG. 11

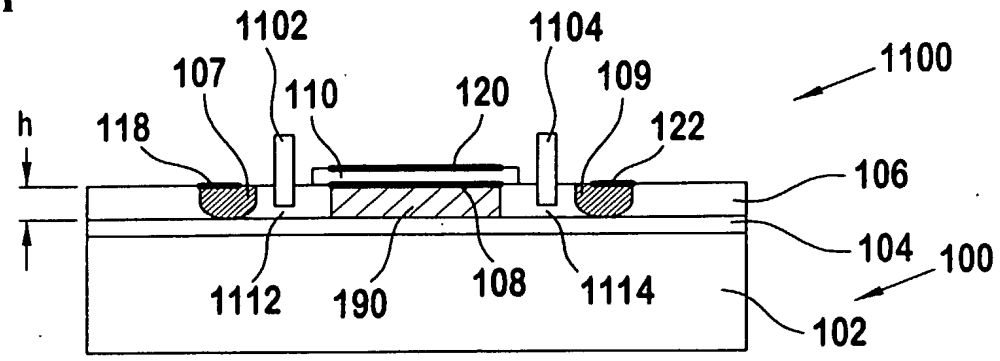


FIG. 12

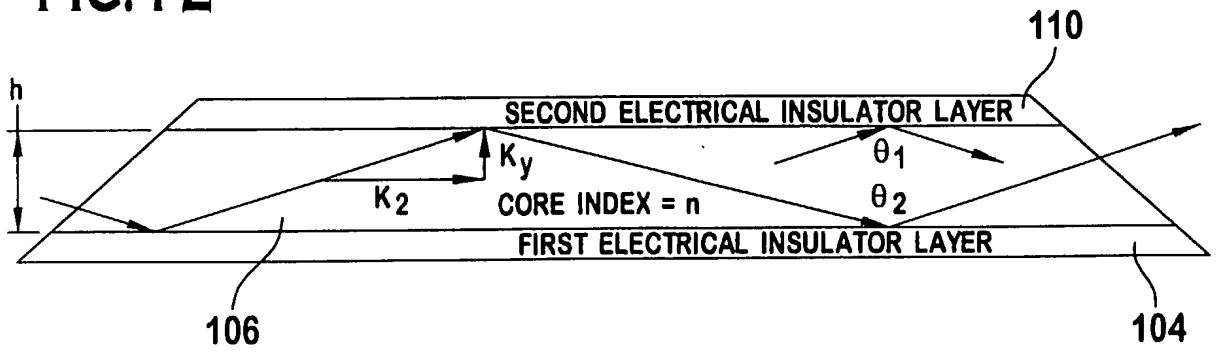


FIG. 13

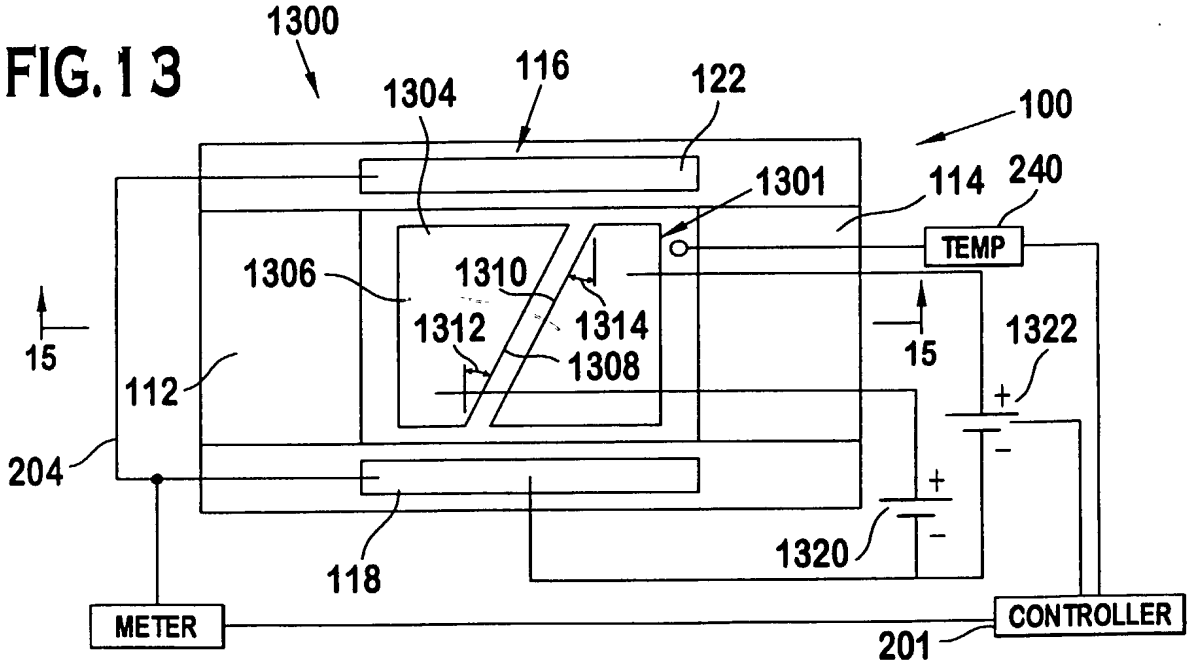


FIG. 20

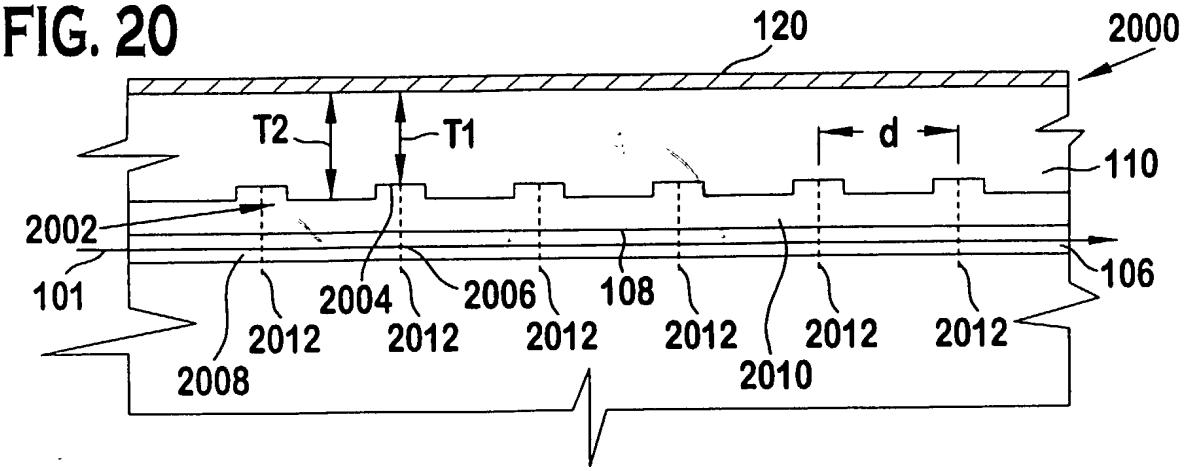


FIG. 21

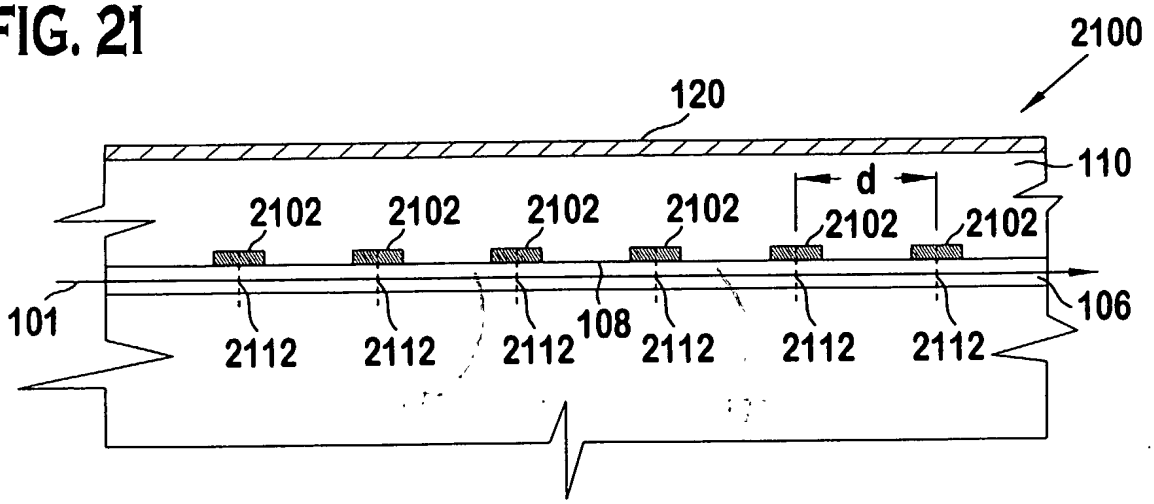


FIG. 22

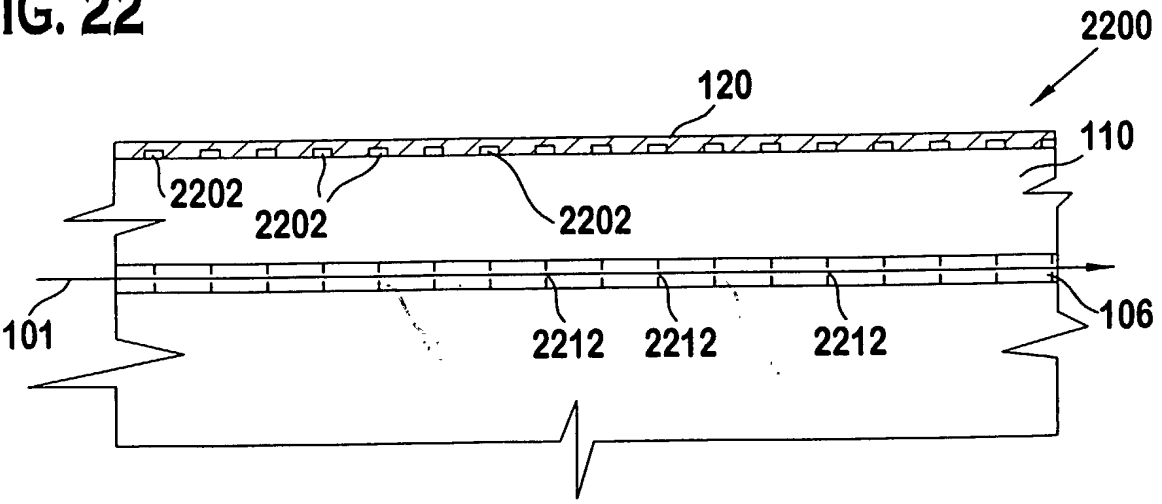


FIG. 30

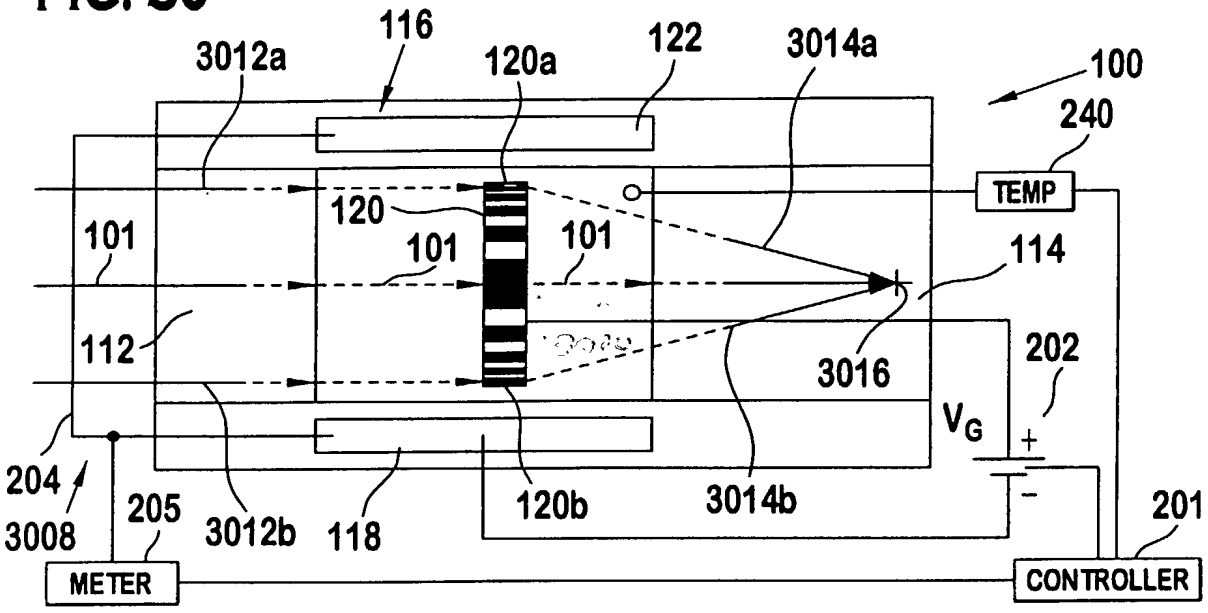
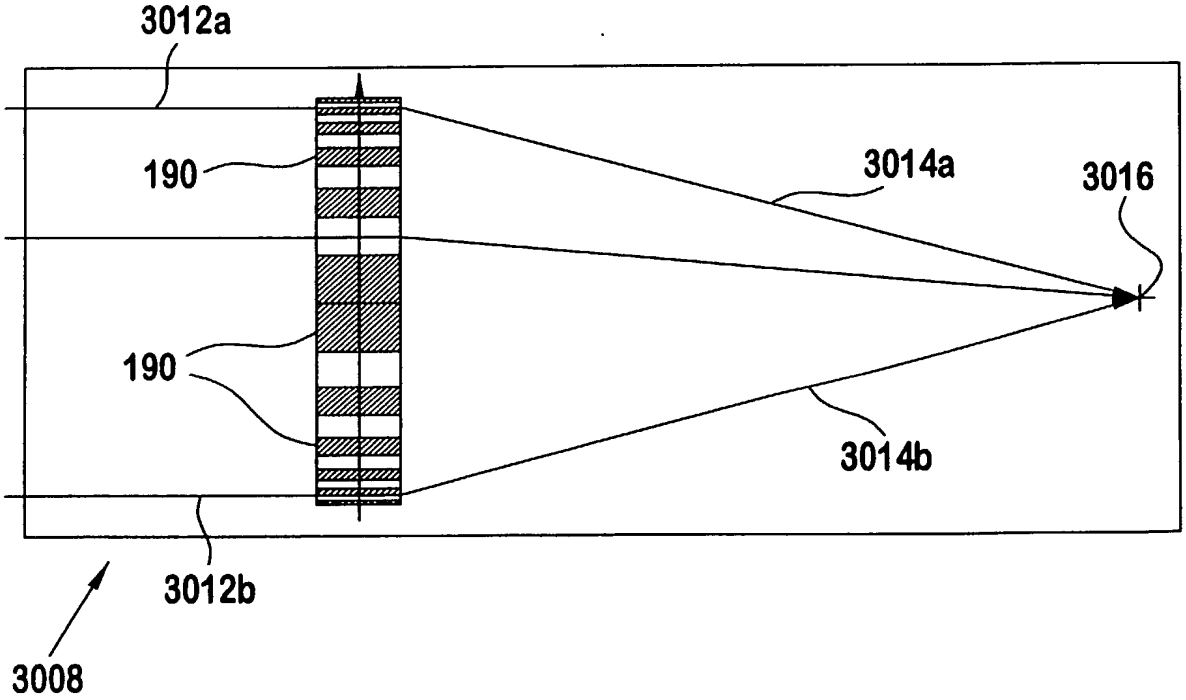


FIG. 30A



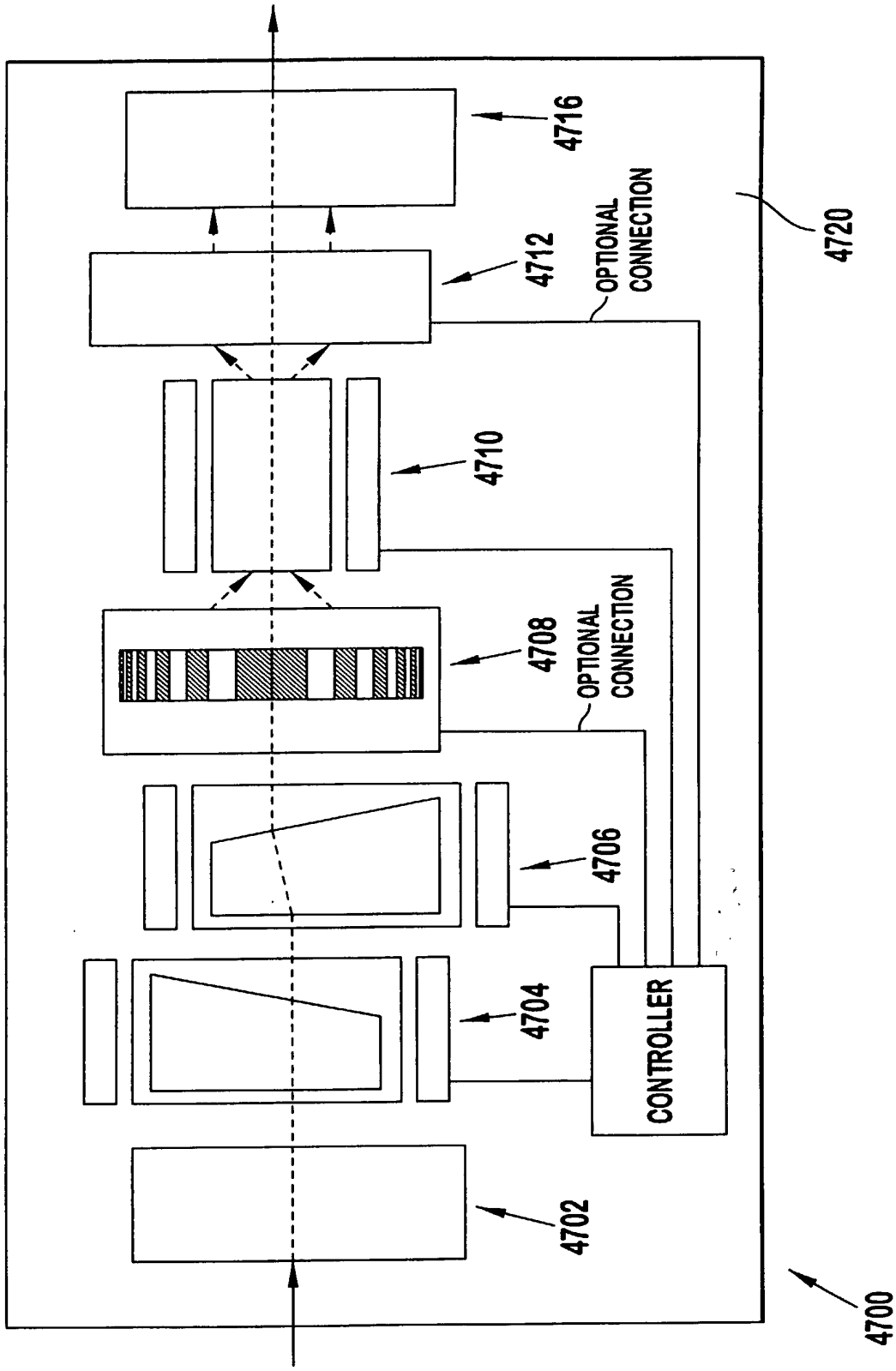

4716
4712
OPTIONAL CONNECTION
4720
4710
4708
OPTIONAL CONNECTION
4706
4704
CONTROLLER
4702
4700

FIG. 47

FIG. 51

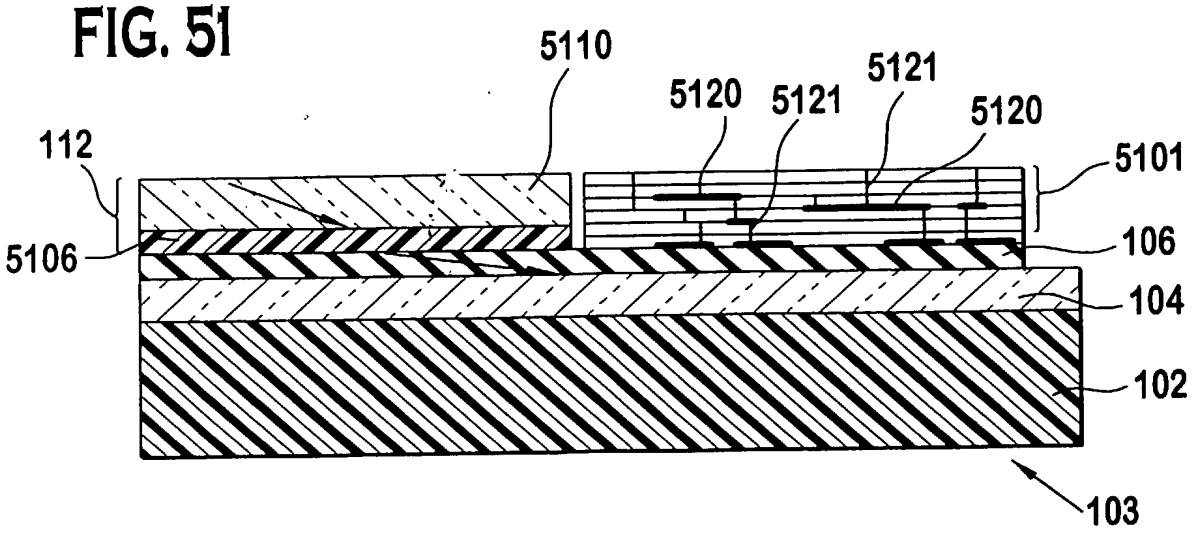
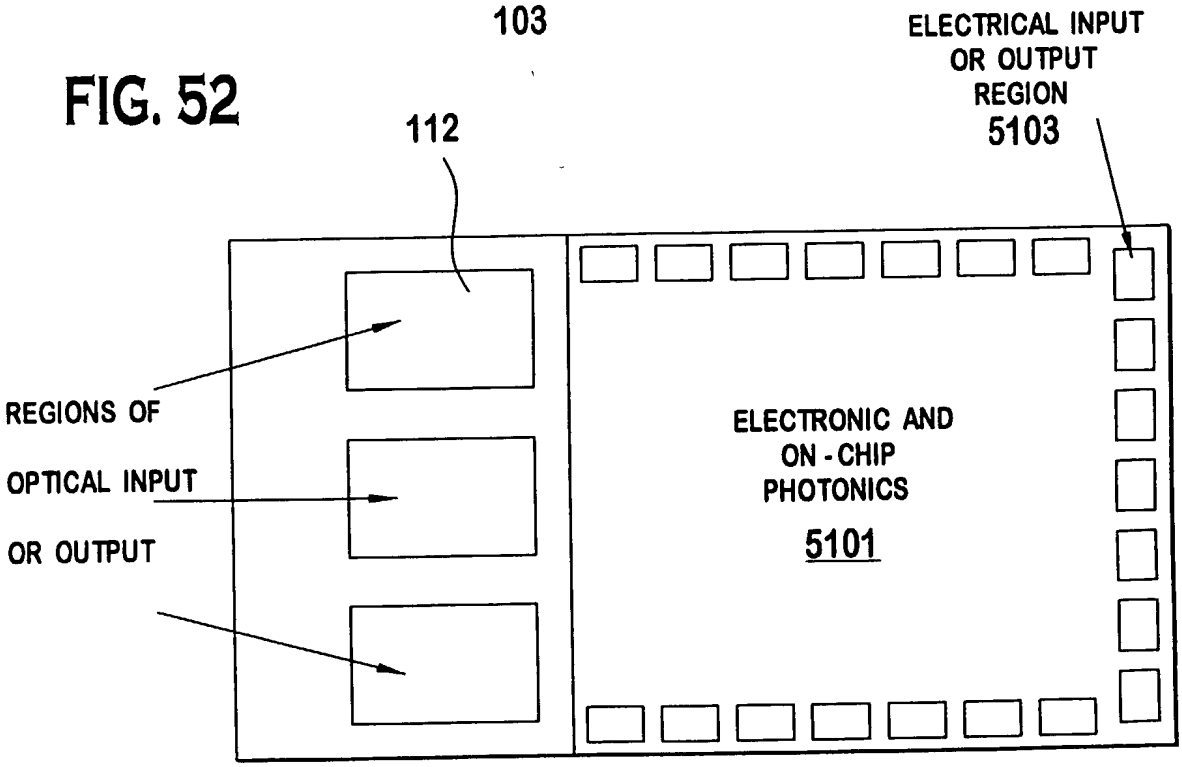

5110
5120
5121
5121
5120
112
5101
5106
106
104
102
103

FIG. 52


103
ELECTRICAL INPUT
OR OUTPUT
REGION
5103
112
REGIONS OF
OPTICAL INPUT
OR OUTPUT
ELECTRONIC AND
ON - CHIP
PHOTONICS
5101

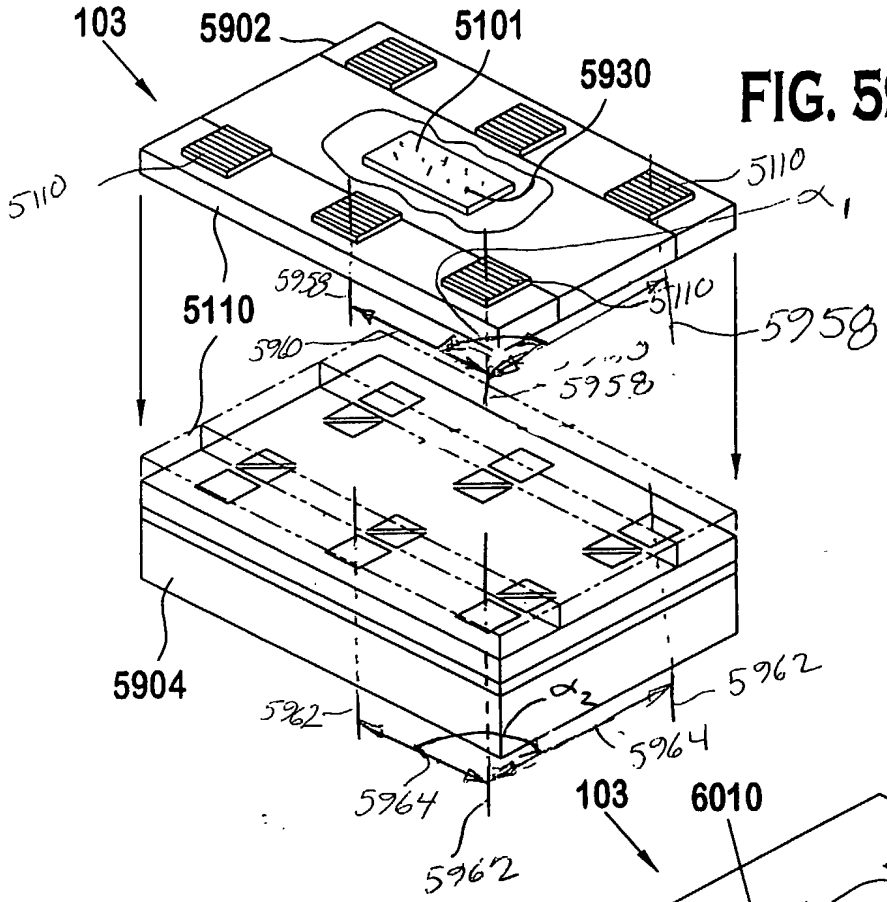


FIG. 59

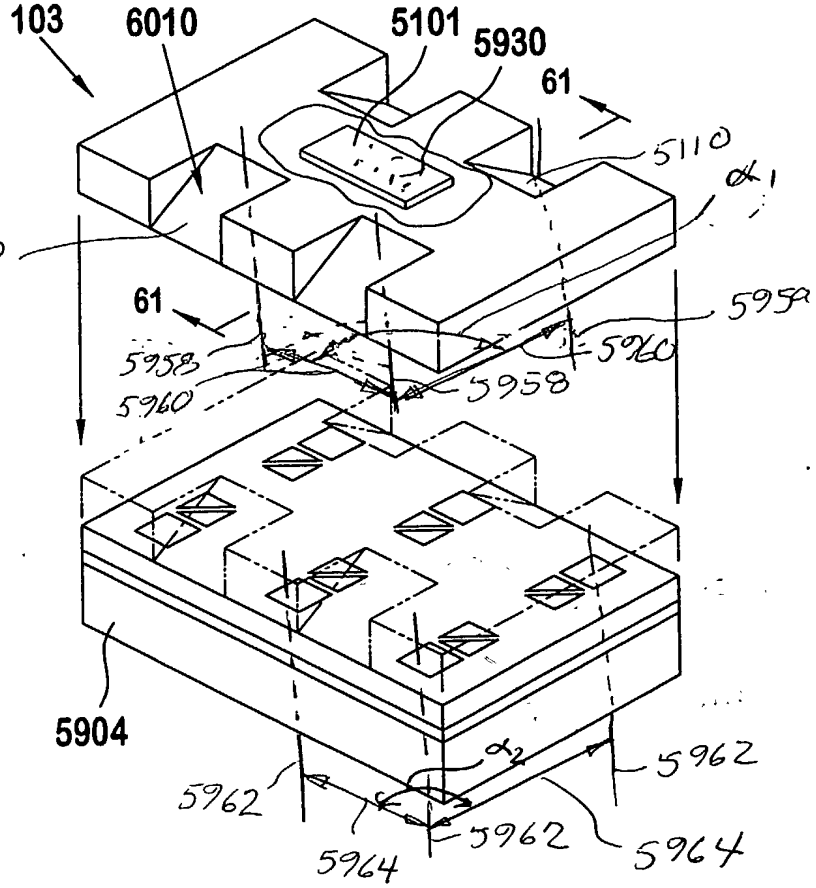


FIG. 60

FIG. 61

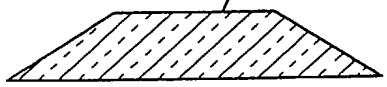


FIG. 62

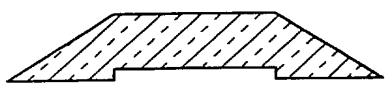


FIG. 67

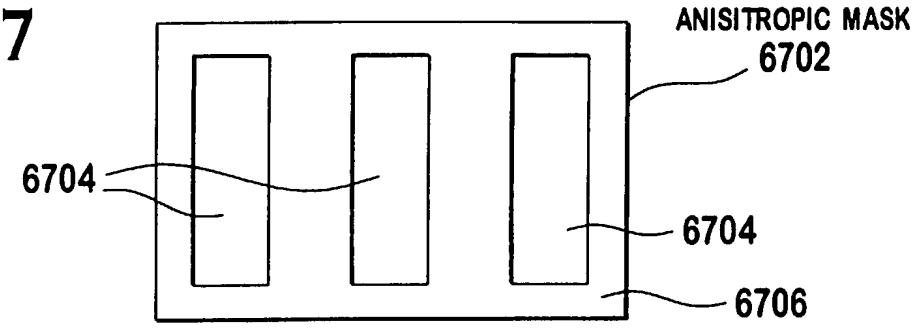


FIG. 68A

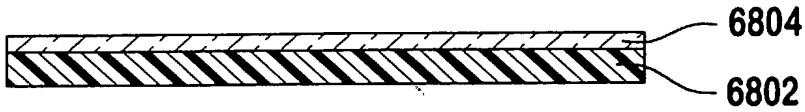


FIG. 68B

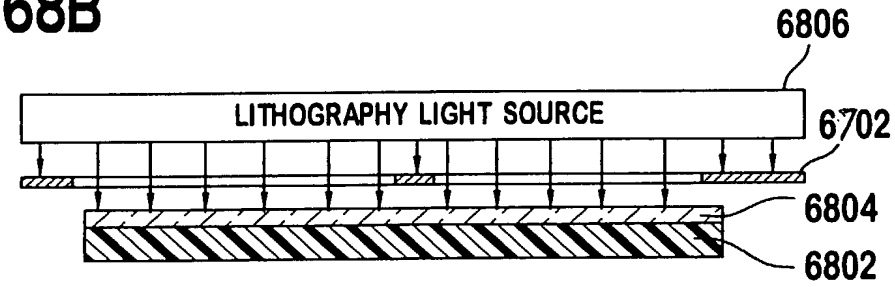
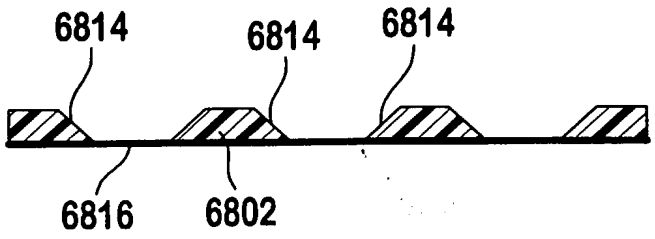


FIG. 68C

FIG. 68D



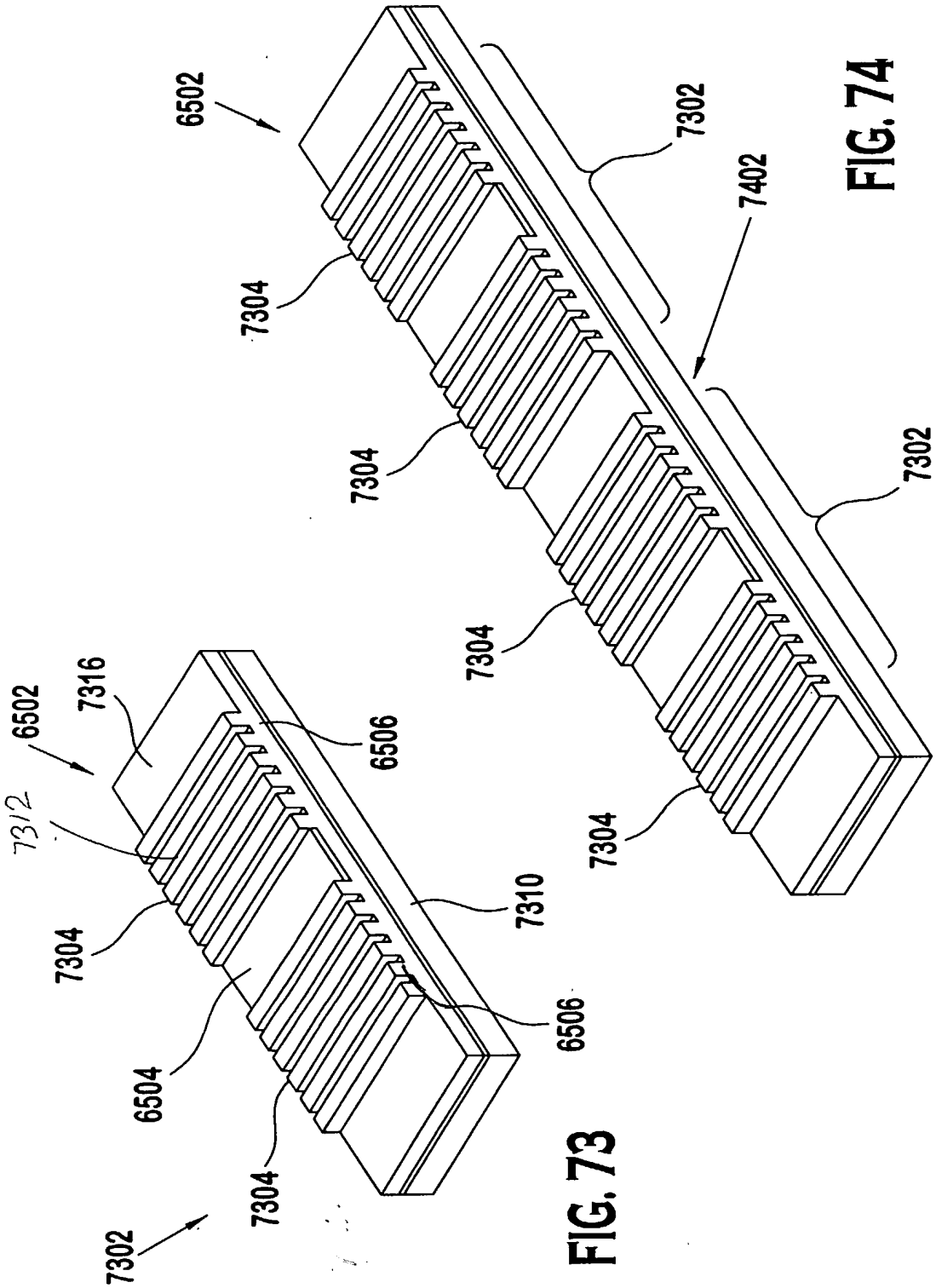

6502
7316
6506
7312
7304
7310
6504
6506
7304
7302

FIG. 73

6502
7302
7402
7304
7304
7302
7304

FIG. 74

FIG. 75

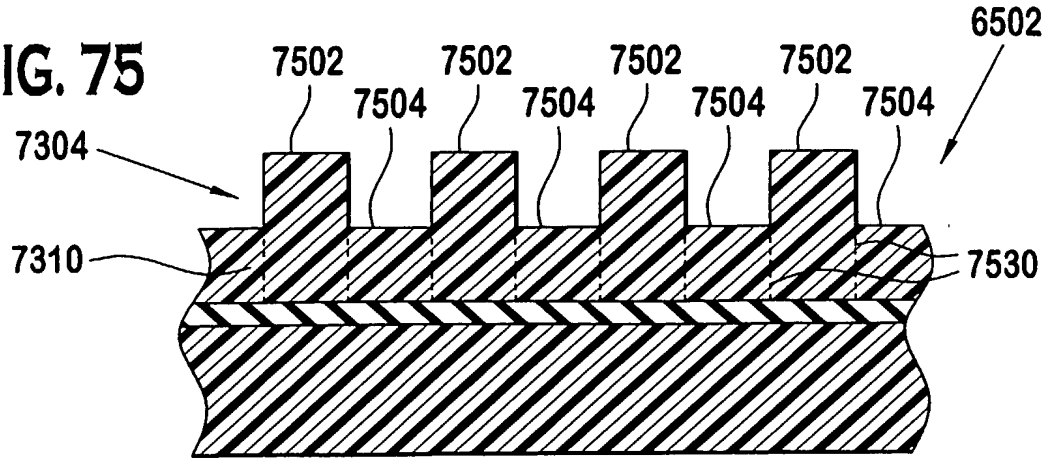


FIG. 76

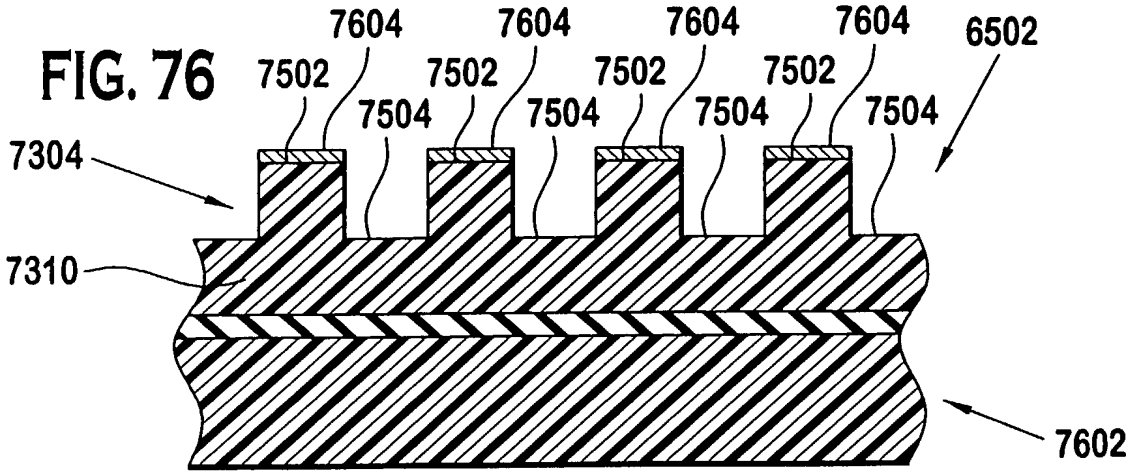
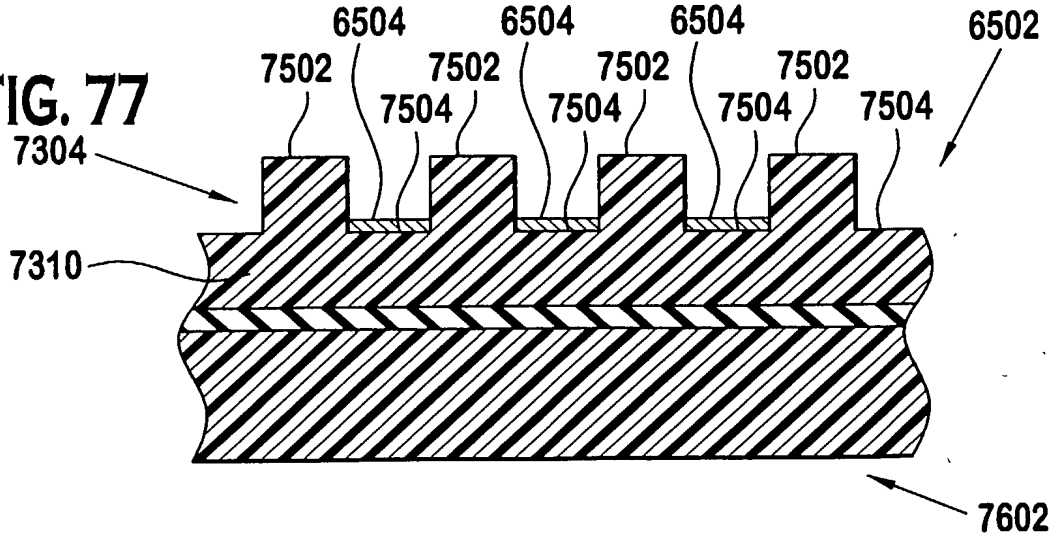


FIG. 77



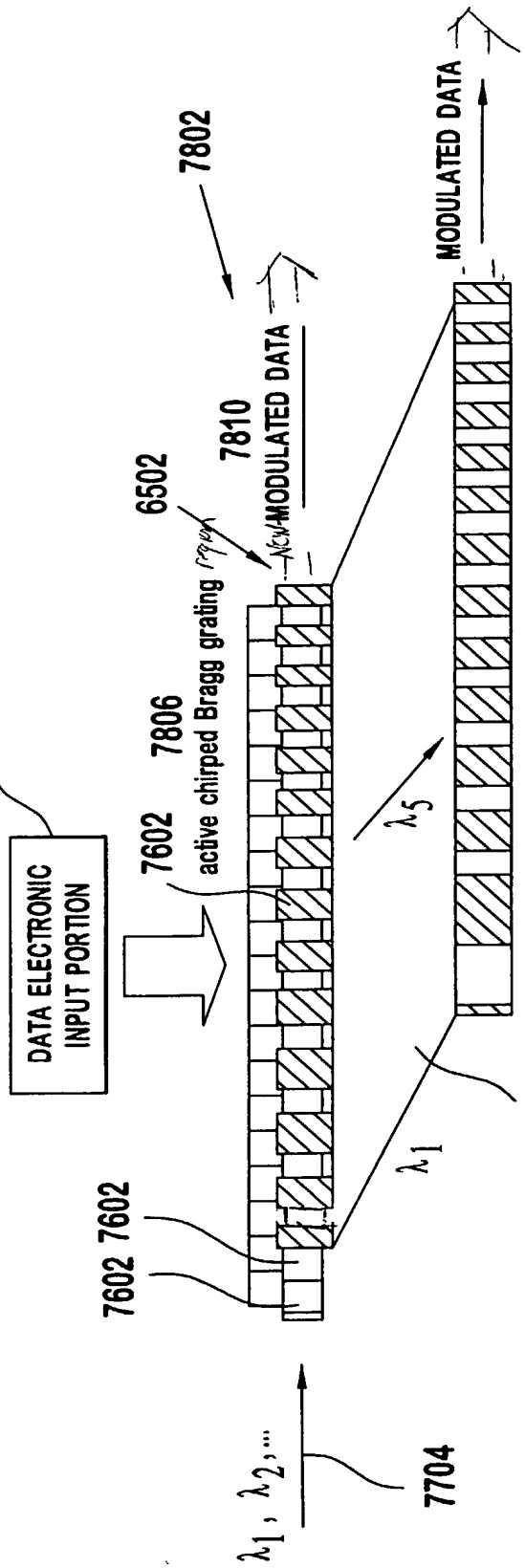
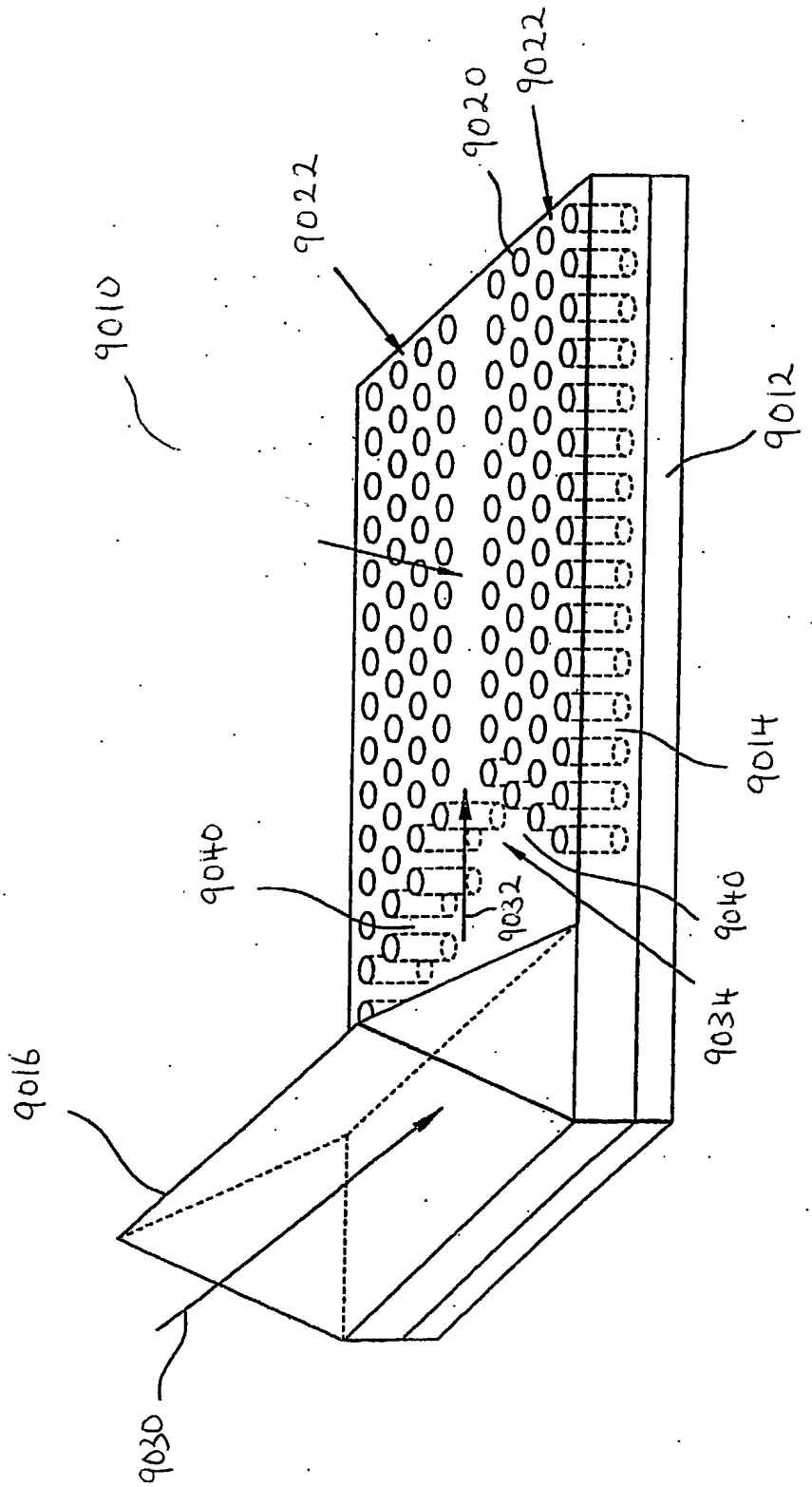
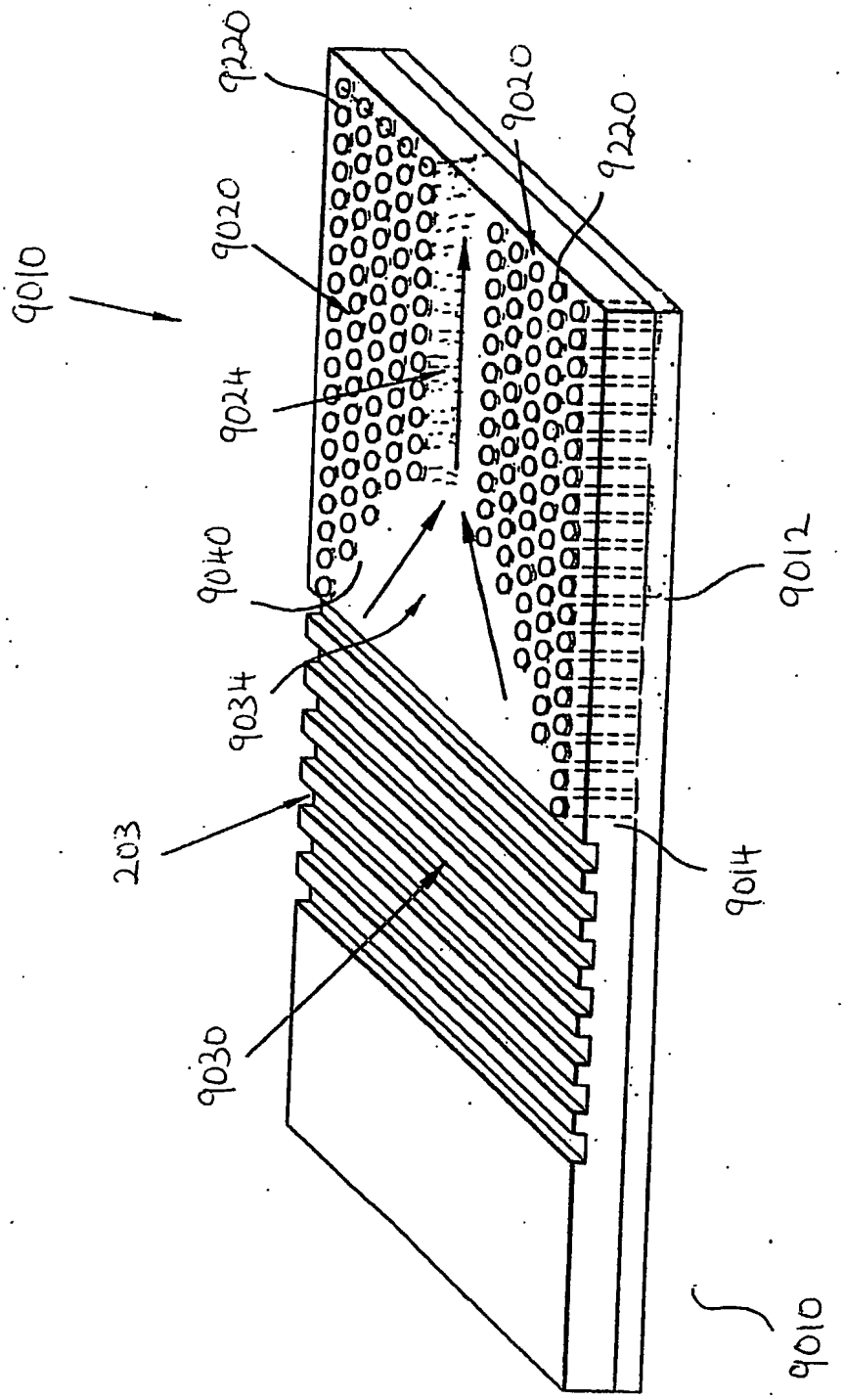

7816
DATA ELECTRONIC INPUT PORTION
7602
7806
active chirped Bragg grating region
6502
7810
NEW MODULATED DATA
7802
MODULATED DATA
passive chirped Bragg grating region
7814
7812
7602 7602
7704
$\lambda_1, \lambda_2, \ldots$
λ_5
λ_1

FIG. 78

FIG. 82




9010
9220
9020
9220
9020
9024
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203
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9012
9014
9010

FIG. 83

FIG. 89